

COMPAL CONFIDENTIAL

MODEL NAME : EDI73

PCB NO : DA8001G1000

BOM P/N : 431AE131L01

WHL-U+MEC1416

2018-10-30

REV : 1.0 (A00)

@ : Un-pop Component

DIS@ : GPU Support

N3@/V3@ : Inspiron/Vostro

WHL@/CNL@ : WHL/CNL

10W@/12P5W@:WHL 10W/12.5W

BASE@/PREM@ : Pentium,Celeron/i3,i5,i7

EXO@/TOPAZ@ : R17M-M1-30/R17M-M2-50

EC@ : EC Support

JP@/PJP@ : JUMP

100@/1000@: Lan

EMI@/ESD@/RF@ : EMI, ESD and RF Component

@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component

CMC@ : XDP Component

CONN@ : Connector Component

KBBL@ : KB Backlight

TPM@/FTPM@ : HW TPM/SW TPM

750_CTPM@:750 and china TPM

ST_CTPM@:ST and china TPM

CTPM@:China TPM

FFS@ : Free Fall Sensor

TYPEC@ : TypeC

TYPEC@EMI@/TYPEC@ESD@: EMI, ESD ,TypeC Component

M1_30@/M2_50@ : R17M-M1-30/R17M-M2-50

2G_G5@/2G_H@/2G_S@/2G_M@ : VRAM type

PCB@/PCB_R1@/PCB_R3_G@/PCB_R3_T@/PCB_R3_H@/PCB_R3_TM@: PCB MB

CPU R1

UC1
SA0000C6R0L
WHL_2.1G_QS@
S IC A31 FJ8068404064702 QQK9 W0 2.1G

UC1
SA0000C6Q0L
WHL_1.6G_QS@
S IC A31 FJ8068404064604 QQTG W0 1.6G

UC1
SA0000C6P0L
WHL_1.8G_QS@
S IC A31 FJ8068404064403 QQK6 W0 1.8G

UC1
SA0000C6Q1L
WHL_I5_12P5@
S IC A31 FJ8068404064604 QQTH W0 1.6G

UC1
SA0000C6R1L
WHL_I3_12P5@
S IC A31 FJ8068404064702 QQKA W0 2.1G

CPU R3

UC1
SA0000C6R3L
WHL_2.1G_R3@
S IC FJ8068404064702 SRD1V W0 2.1G A31

UC1
SA0000C6Q3L
WHL_1.6G_R3@
S IC FJ8068404064604 SREJQ W0 1.6G A31

UC1
SA0000C6P2L
WHL_1.8G_R3@
S IC FJ8068404064405 SREJP W0 1.8G A31

UC1
SA0000C6Q5L
I5_12P5_R3@
S IC FJ8068404064604 SREJR W0 1.6G FCBGA 1528 A31

UC1
SA0000C6R5L
I3_12P5_R3@
S IC FJ8068404064702 SRD1V W0 2.1G FCBGA 1528 A31

Layout Dell logo



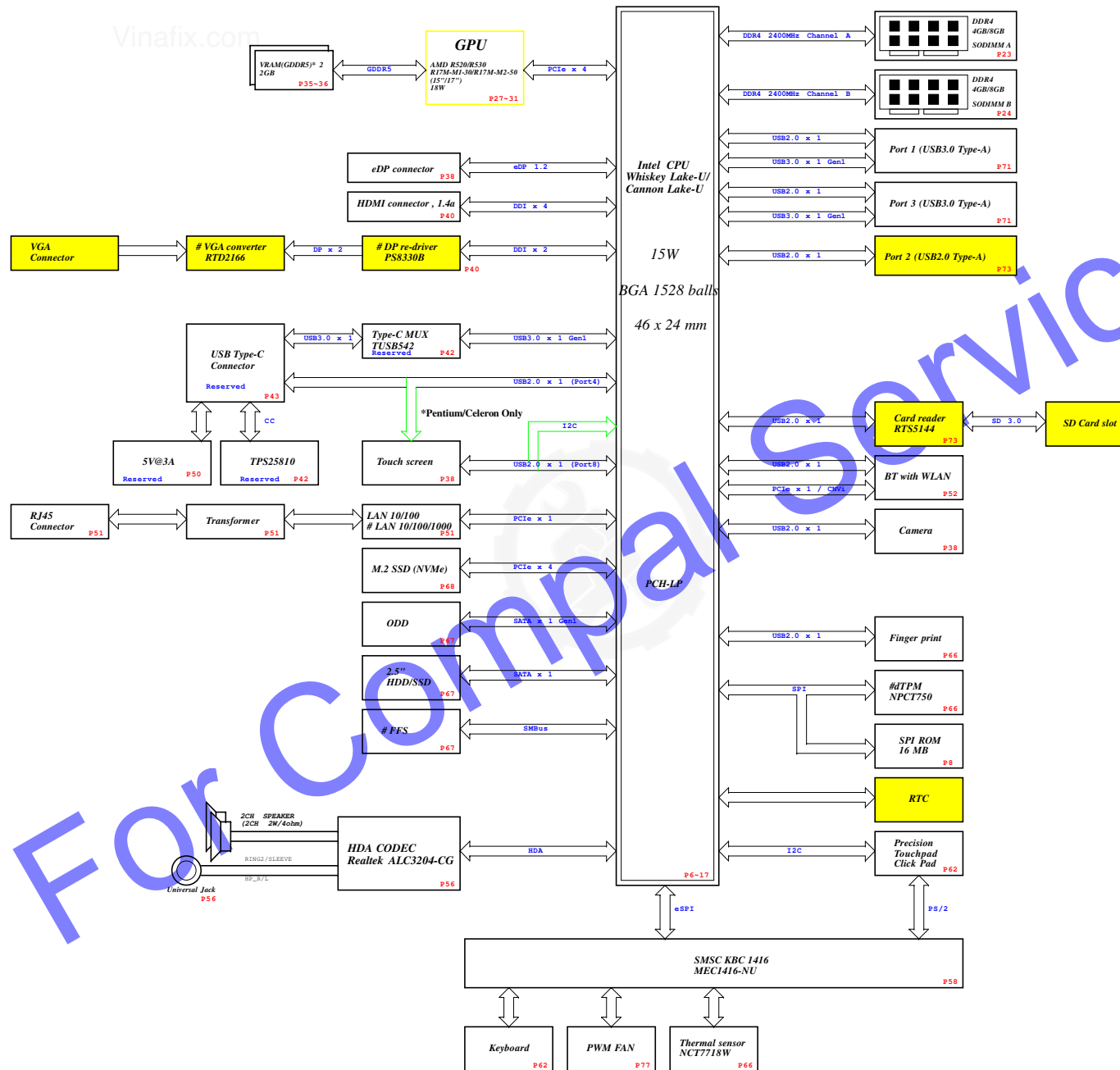
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REV: X01
PWB: 9HTP8

UC1
SA0000C150L
WHL_1.8G_ES2@
S IC A31 FJ8068403999819 QQAT W0 1.8G

UC1
SA0000C160L
WHL_1.6G_ES2@
S IC A31 FJ8068404000016 QQAU W0 1.6G

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Block Diagram



----> V3 only

Battery	RTC
Charger	Daughter board

POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3		LOW	LOW	LOW	ON	OFF	OFF	OFF
G3		OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3		---	---	---	---	---	---	---

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port, IO/B
3	USB2.0 port2
4*	TypeC
5	Finger printer
6	Camera
7	Card reader , IO/B
8*	Touch screen
9	WWAN (Reserved)
10	BT

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A
+RTC_CELL	RTC power	ON	ON	ON
+3VALW_DS	+3VALW power for PCH DSW rails	ON	ON	ON*
+5VALW	System +5V always on power rail	ON	ON	ON*
+3VALW	System +3V always on power rail	ON	ON	ON*
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF
+0.6V_DDR_VTT	DDR +0.6V power rail for DDR terminator	ON	OFF	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF
+VCCIO	+1.05 VCCIO power rail	ON	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF
+1.35V_MEM GFX	+1.35V power rail for GPU	ON	OFF	OFF
+3VGS	+3V power rail for GPU	ON	OFF	OFF
+1.8VGS	+1.8V power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	+0.95V power rail for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Board ID & Model ID Table

#	Pull-down	Pull-up	Voltage	Board ID
1	100	10.0	3.000	EVT
2	100	17.8	2.801	DVT1
3	100	27.0	2.598	DVT2
4	100	37.4	2.402	
5	100	49.9	2.201	Pilot
6	100	64.9	2.001	
7	100	82.5	1.808	
8	100	107.0	1.594	
9	100	154.0	1.299	
10	100	200.0	1.100	

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 port1
USB3.0-2	PCIE-2		WWAN (Reserved)
USB3.0-3	PCIE-3		USB3.0 port2
USB3.0-4	PCIE-4		TypeC
USB3.0-5	PCIE-5		GPU
USB3.0-6	PCIE-6		GPU
	PCIE-7		GPU
	PCIE-8		GPU
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1A	SATA ODD
	PCIE-13		NVME SSD
	PCIE-14		NVME SSD
	PCIE-15	SATA-1B	NVME SSD
	PCIE-16	SATA-2	NVME SSD

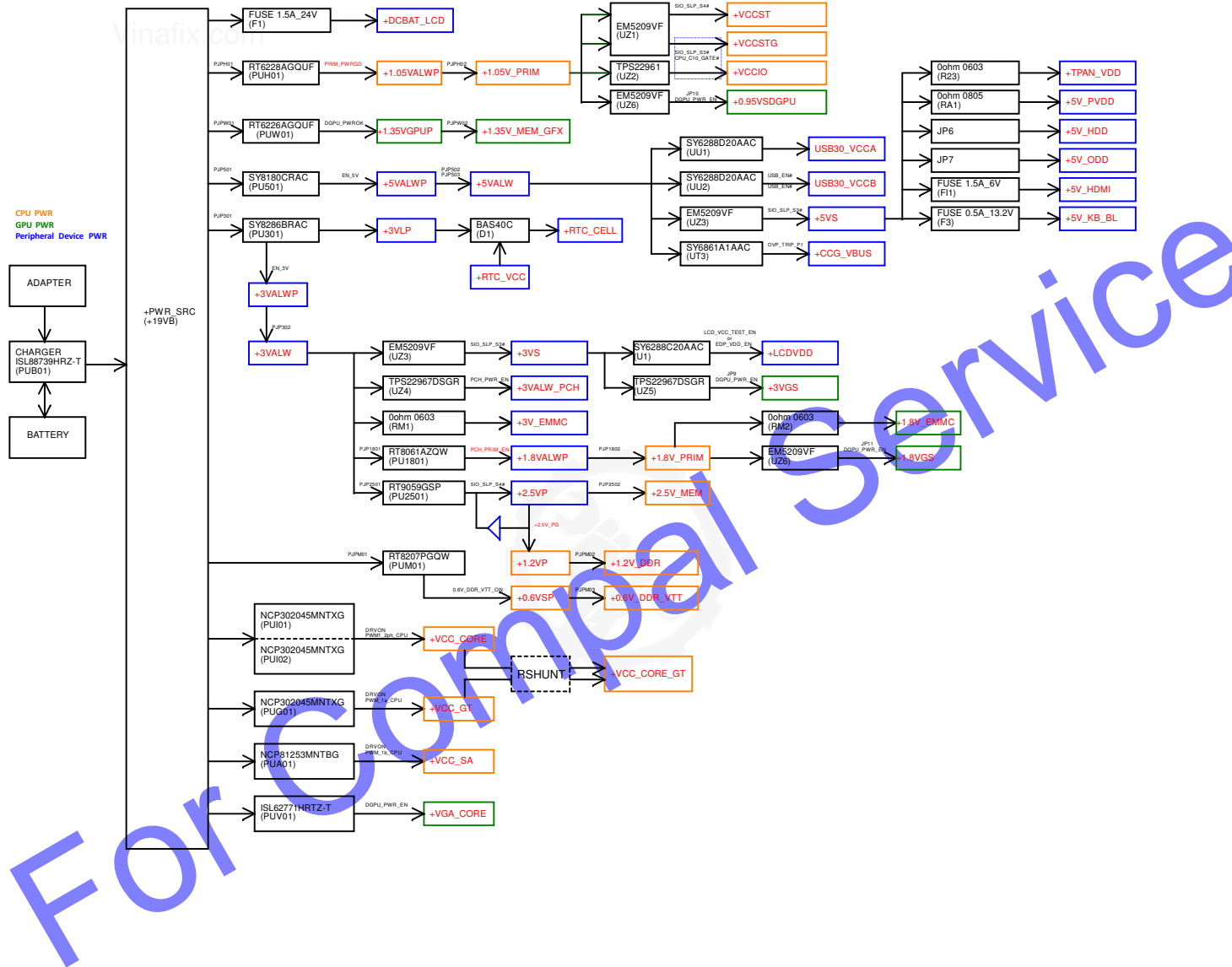
Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIE* #7	PCIE* #8	PCIE* #9	PCIE* #10	PCIE* #11	PCIE* #12	PCIE* #13	PCIE* #14	PCIE* #15	PCIE* #16
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes

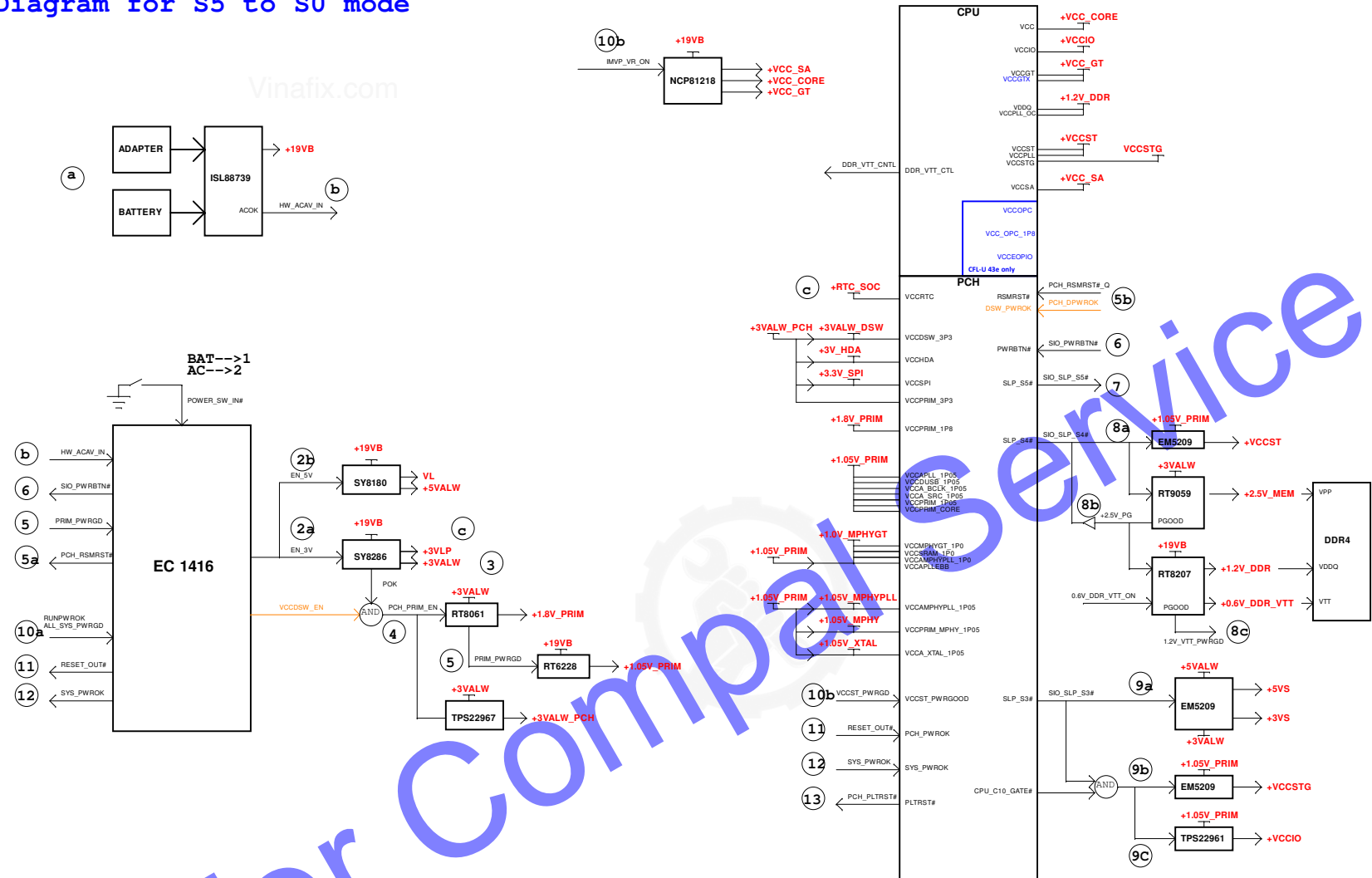
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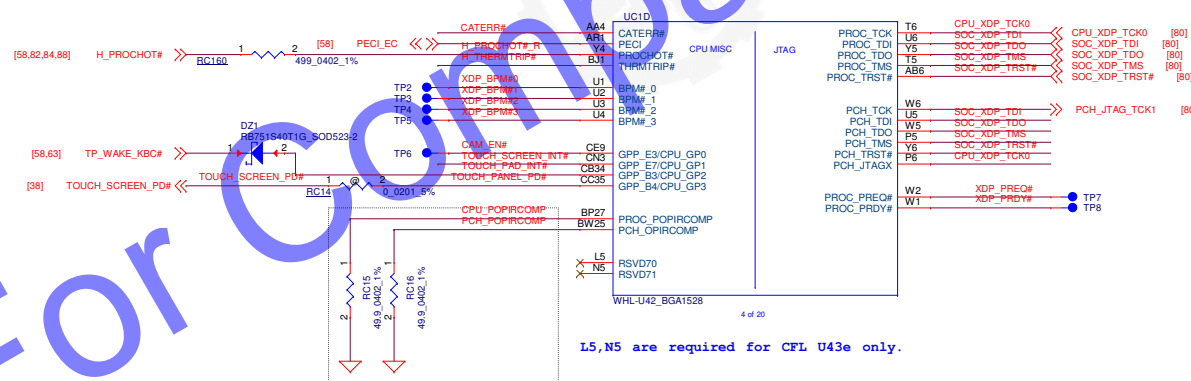
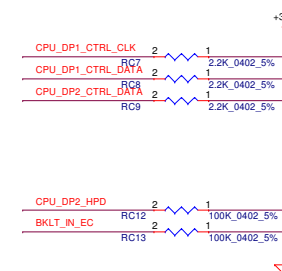
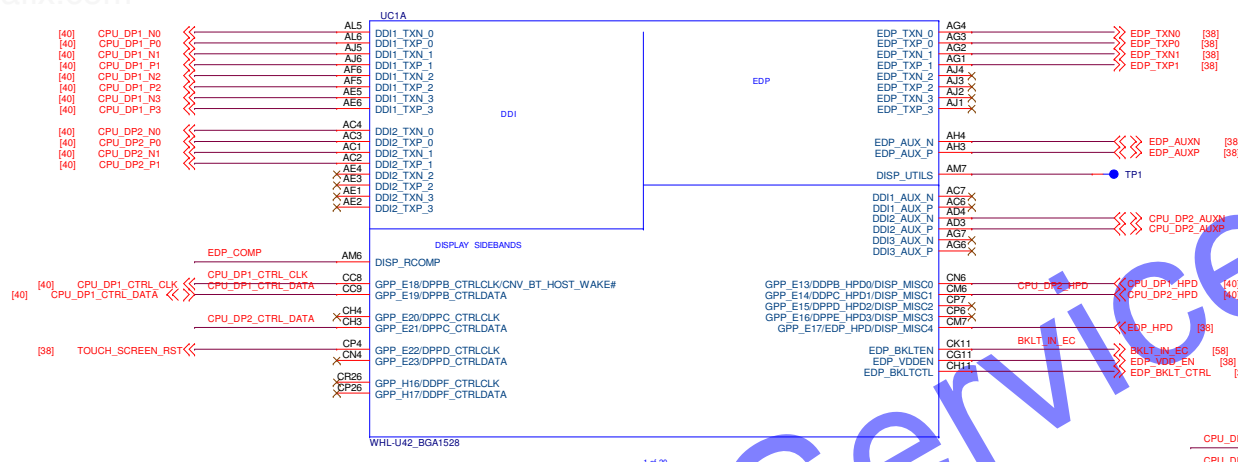
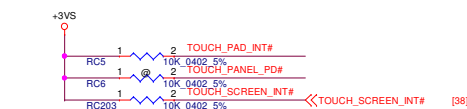


Timing Diagram for S5 to S0 mode



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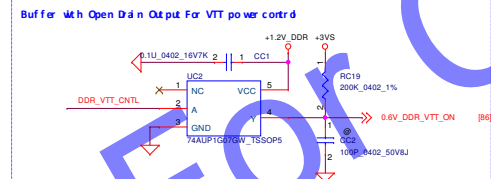
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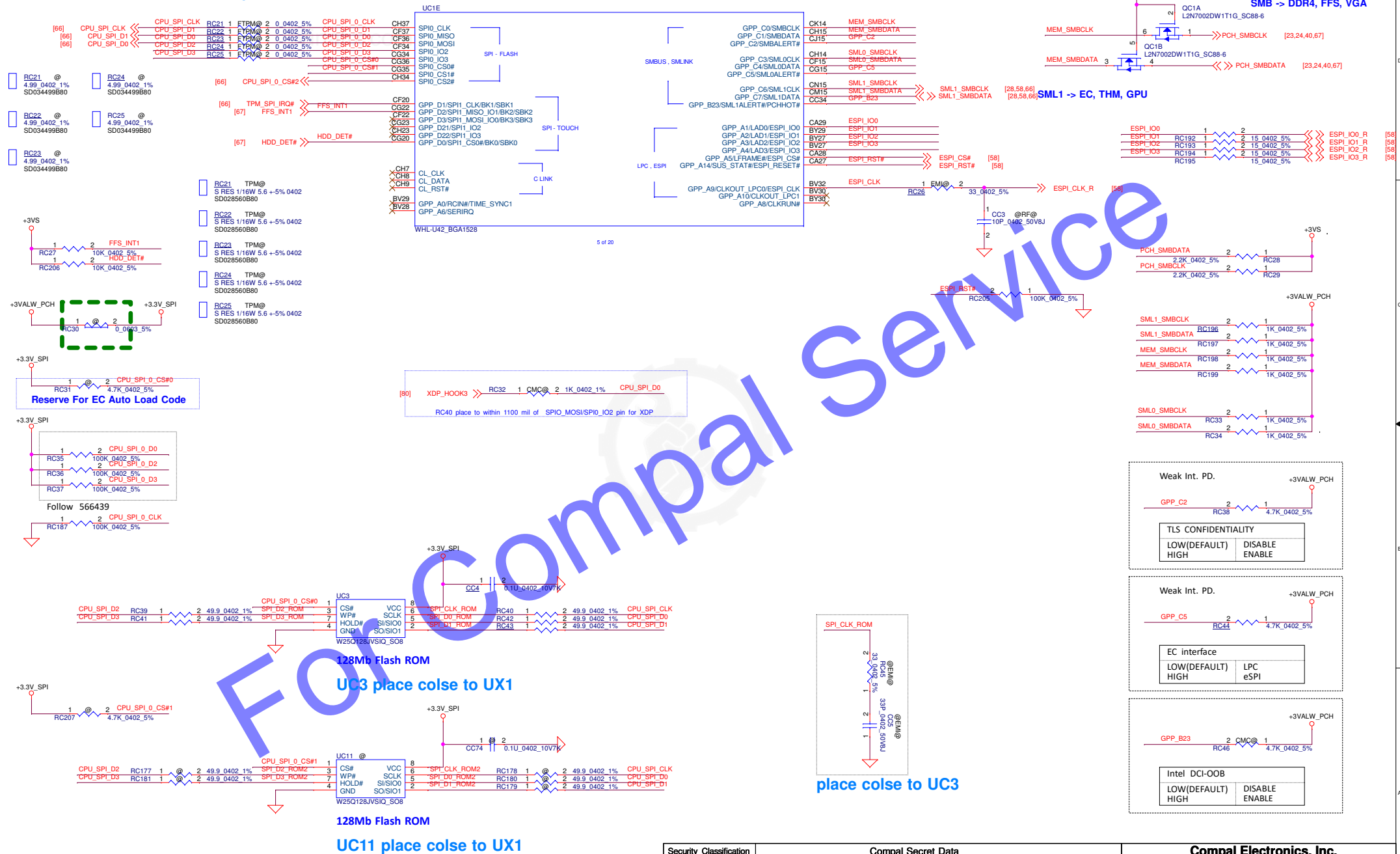
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DDR4 Interleaved Memory

Vinafix.com



RC21~RC25 place colse to Device

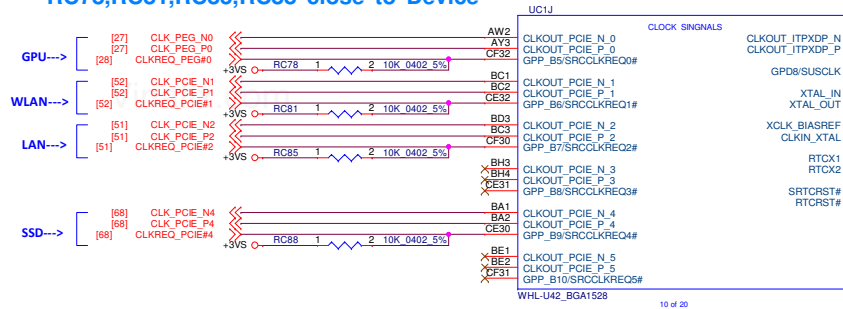


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LOW = ENABLE --> ME lock can't update ME
HIGH = DISABLE --> ME unlock can update ME

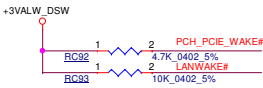
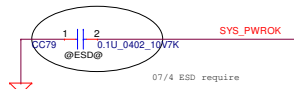
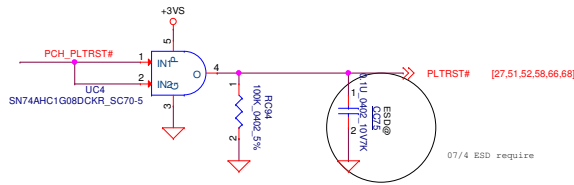
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RC78,RC81,RC85,RC88 close to Device

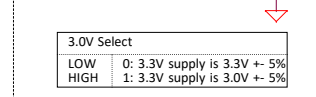
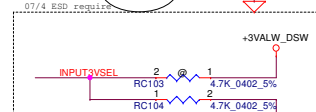
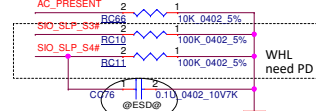
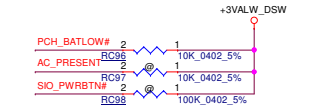
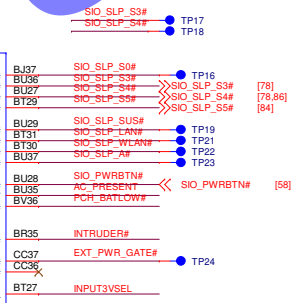
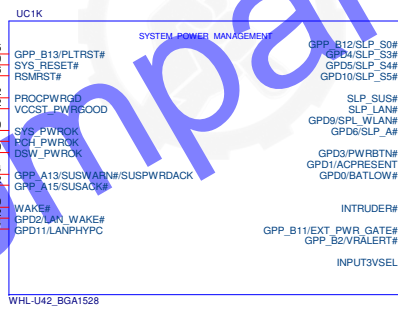
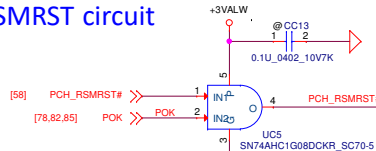


COMPENSATION FOR XCLK_BIASREF
CAD Note:
Min trace width=10 mils, Spacing=15 mils
Max trace length=1000 mils

PCH_PLTRST#

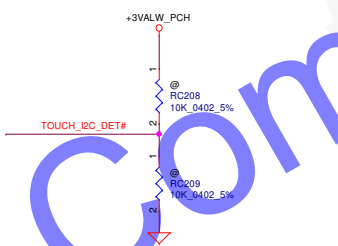
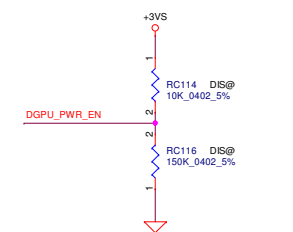
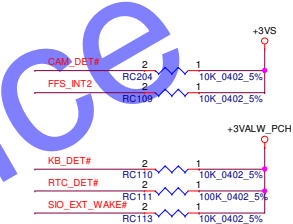
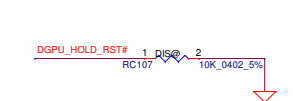
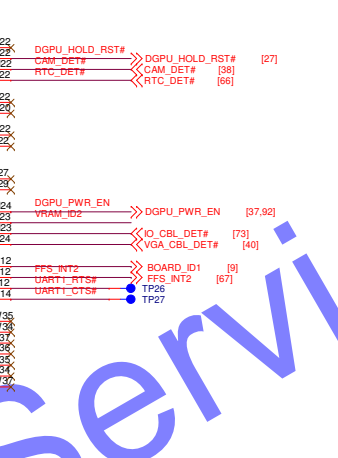
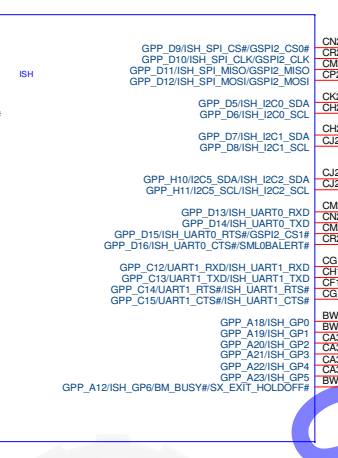
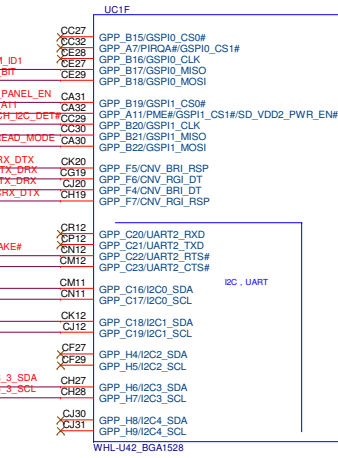
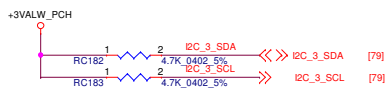
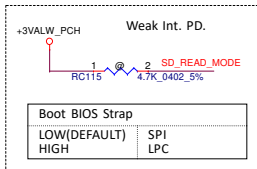
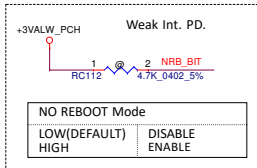
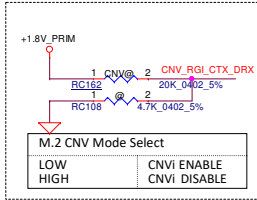
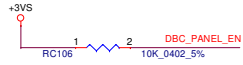
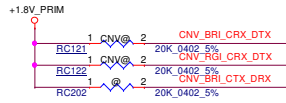


RSMRST circuit

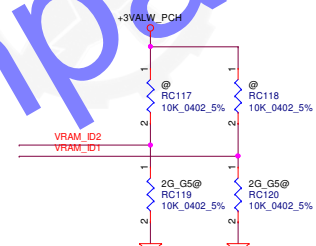


3.0V Select	
LOW	0: 3.3V supply is 3.3V +/- 5%
HIGH	1: 3.3V supply is 3.0V +/- 5%

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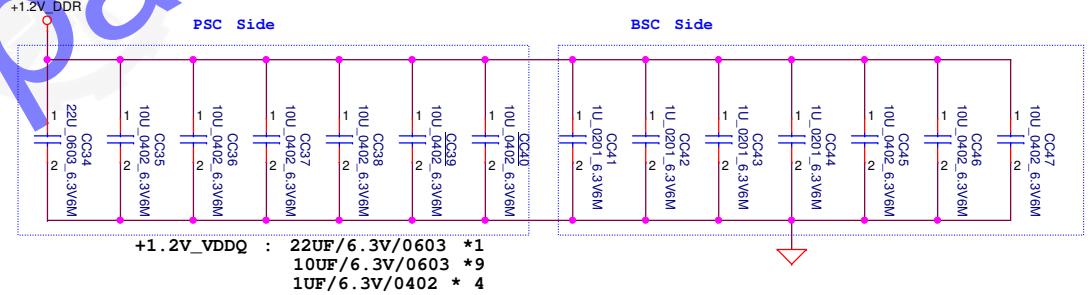
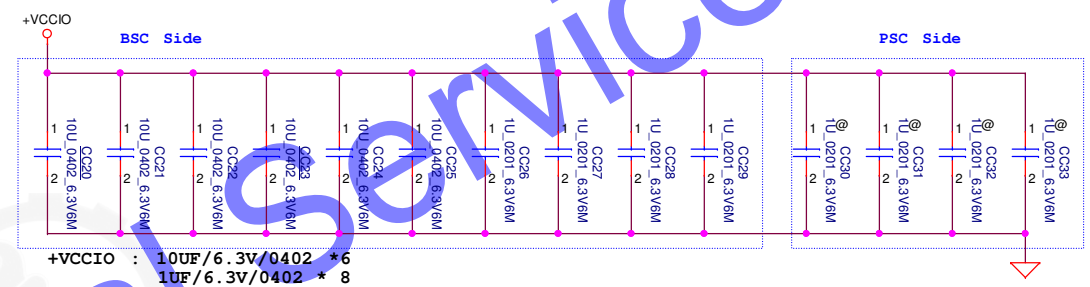
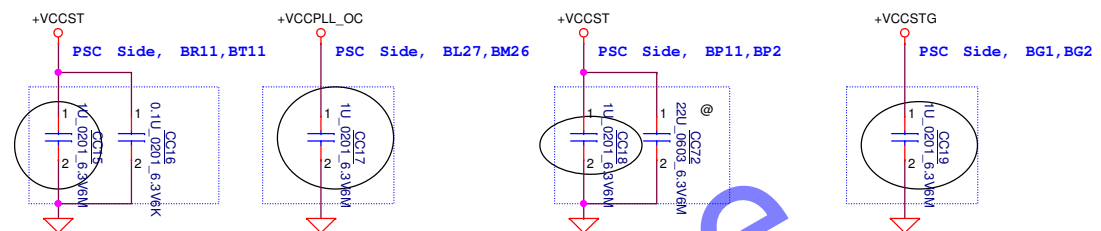
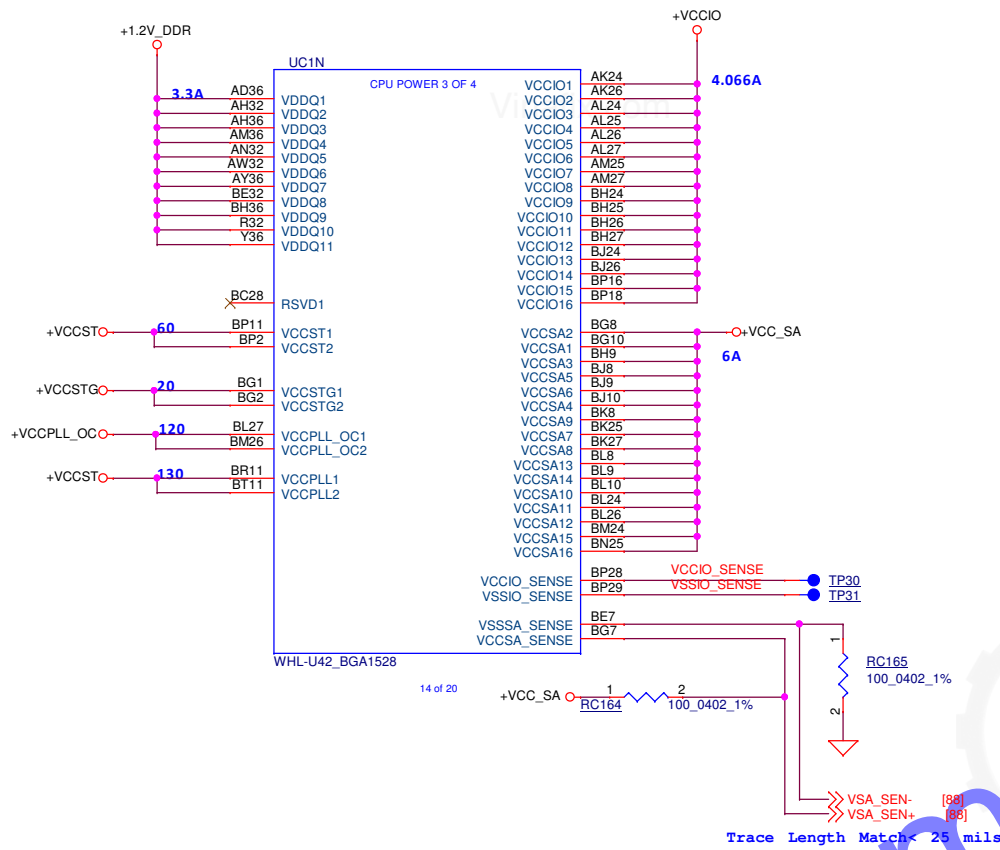


RC208,RC209 Touch panel interface	
LOW	I2C
HIGH	USB



VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_CN23)	VBIOS_ID1 (GPP_CE27)
2G GDDR5	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

For Compal Service

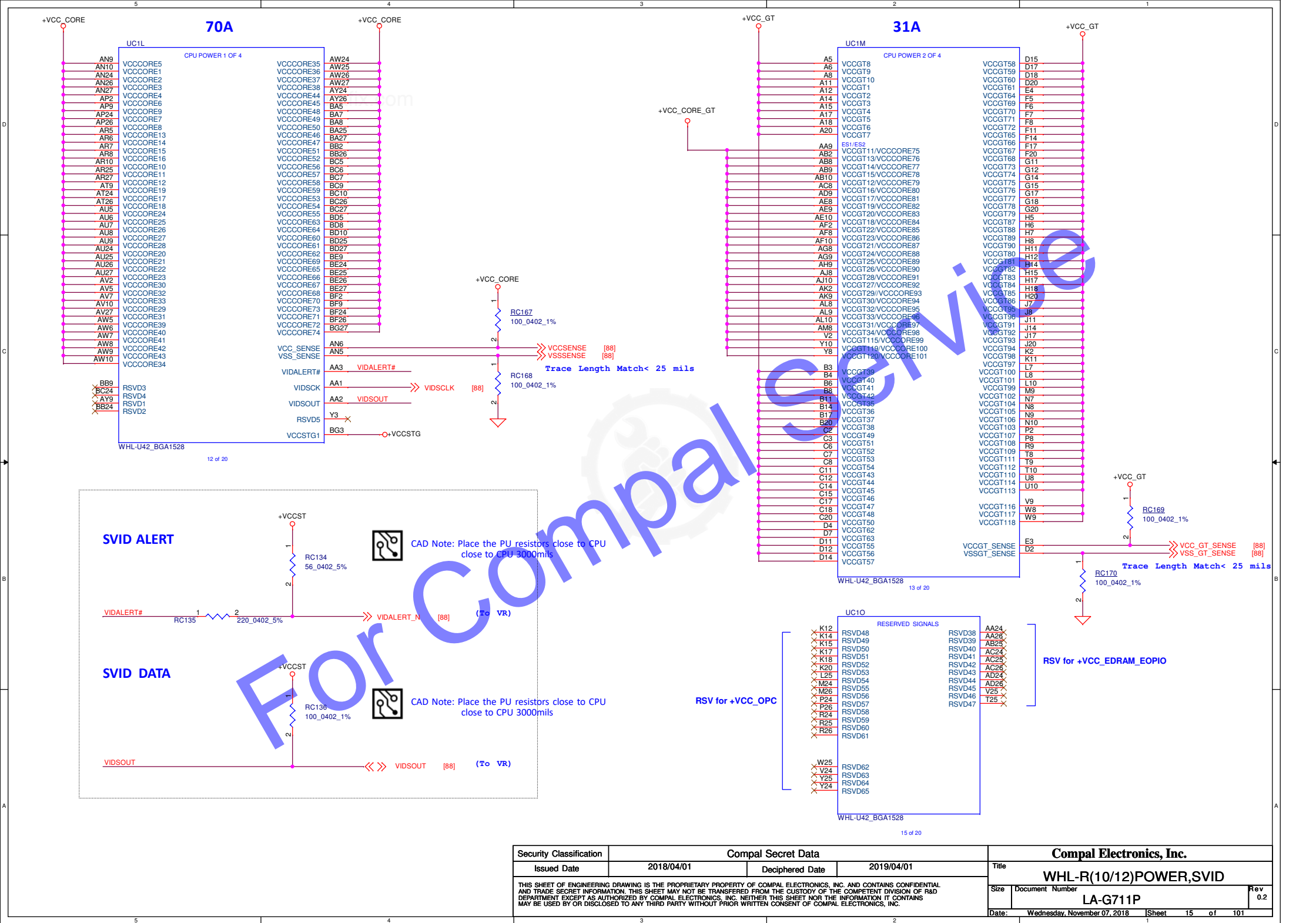


Trace Length Match< 25 mils

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										WHL-U(8/12)POWER	
										Size	
										Document Number	
										LA-G711P	
										Date:	
										Wednesday, November 07, 2018	
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										of	
										101	

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						Size		Document Number		Rev	
						LA-G711P		0.2			
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Reset sequence after PCU PLL is locked	
CFG0	1 : (DEFAULT) Normal Operation No Stall 0 : Stall

PCI Express Static Lane Reversal For All PEG Ports	
CFG2	1 : (DEFAULT) Normal Operation 0 : Lane Reversal

Display Port Presence Strap	
CFG4	0 : Enabled; An external Display Port device is connected to the Embedded Display Port 1 : Disabled; No Physical Display Port attached to Embedded Display Port

PCI Express Bifurcation	
CFG[6:5]	<ul style="list-style-type: none"> 00 = 1x8 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*

PEG Training	
CFG7	1 : (default) PEG Train immediately following RESET# de-assertion 0 : PEG Wait for BIOS for training.



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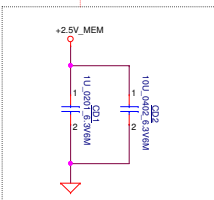
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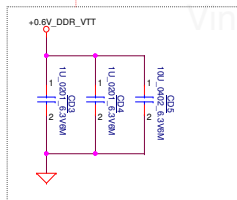
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Main Func = DDR

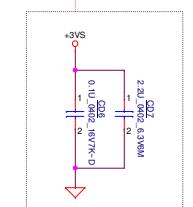
Layout Note:
Place near JDIMM1.257,259



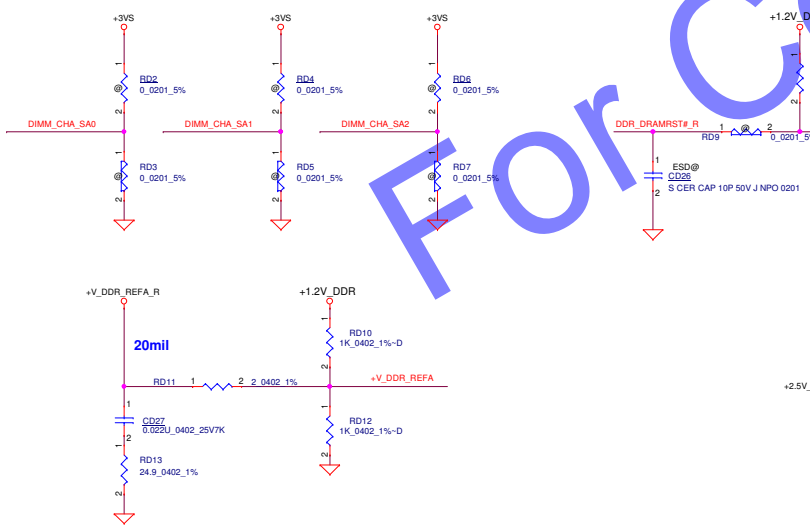
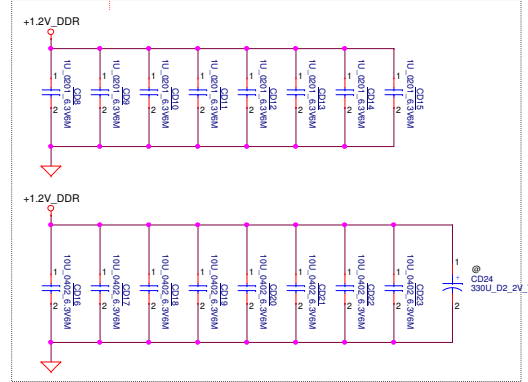
Layout Note:
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Layout Note:
Place near JDIMM1.255



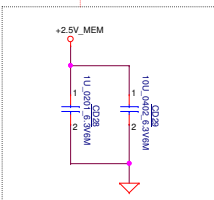
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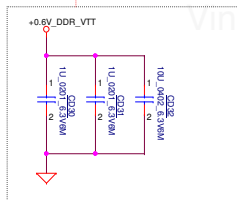
All VREF traces should
have 10 mil trace width

Main Func = DDR

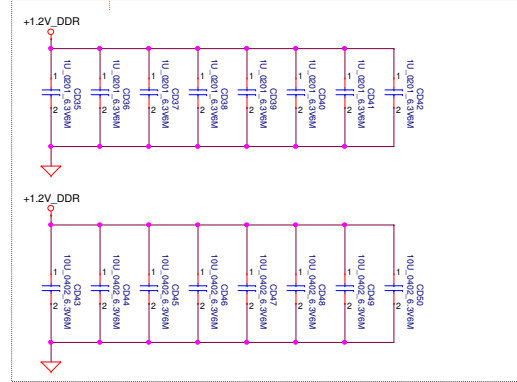
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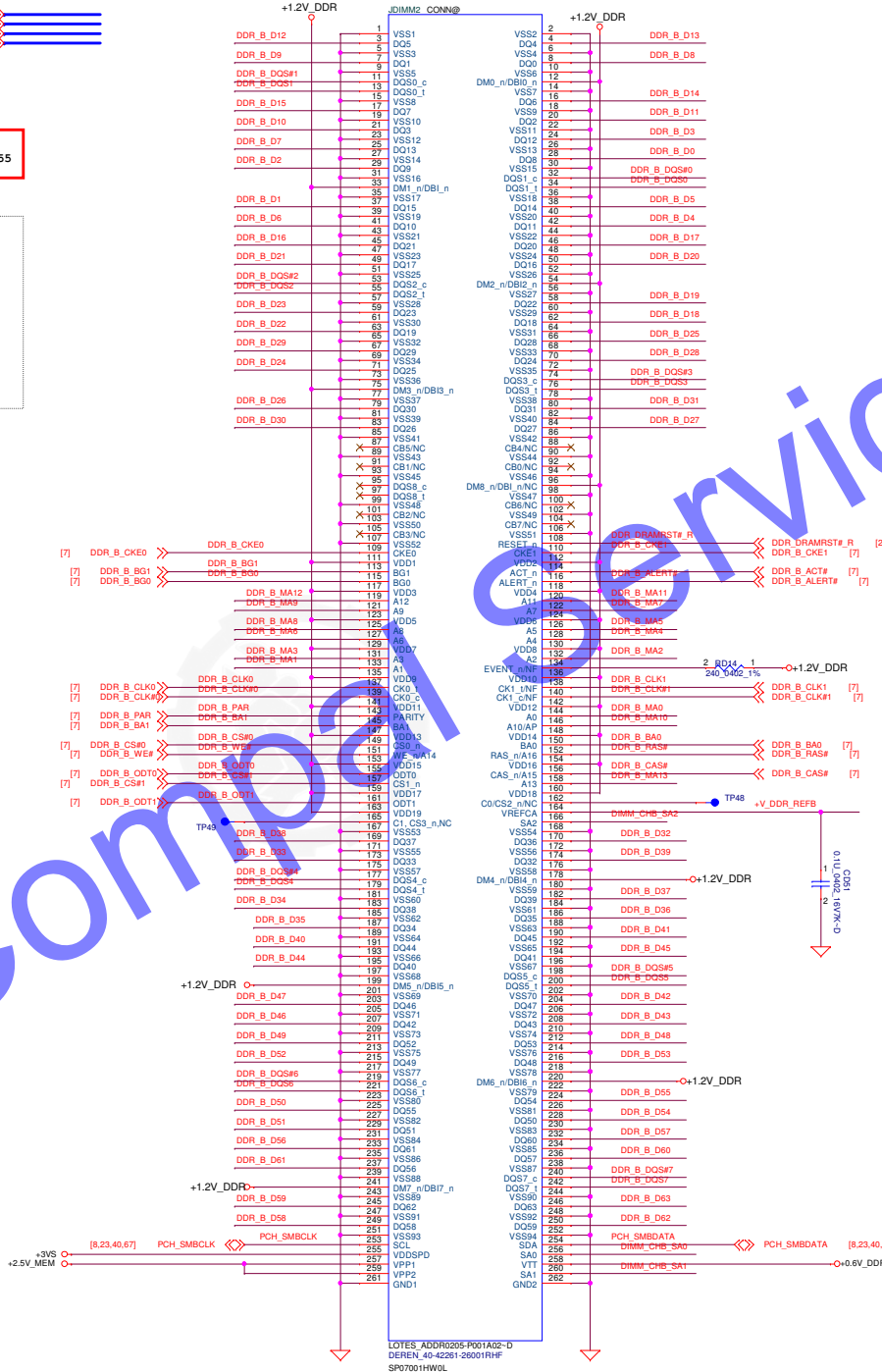
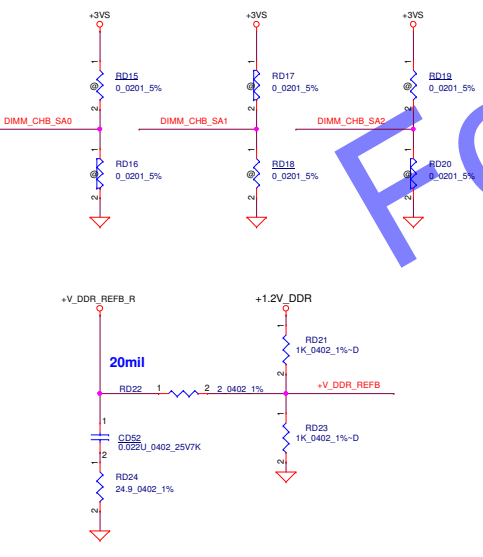
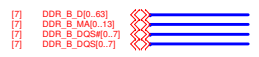
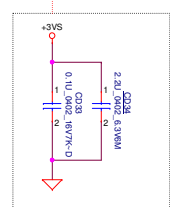
Layout Note:
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Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.255



All VREF traces should
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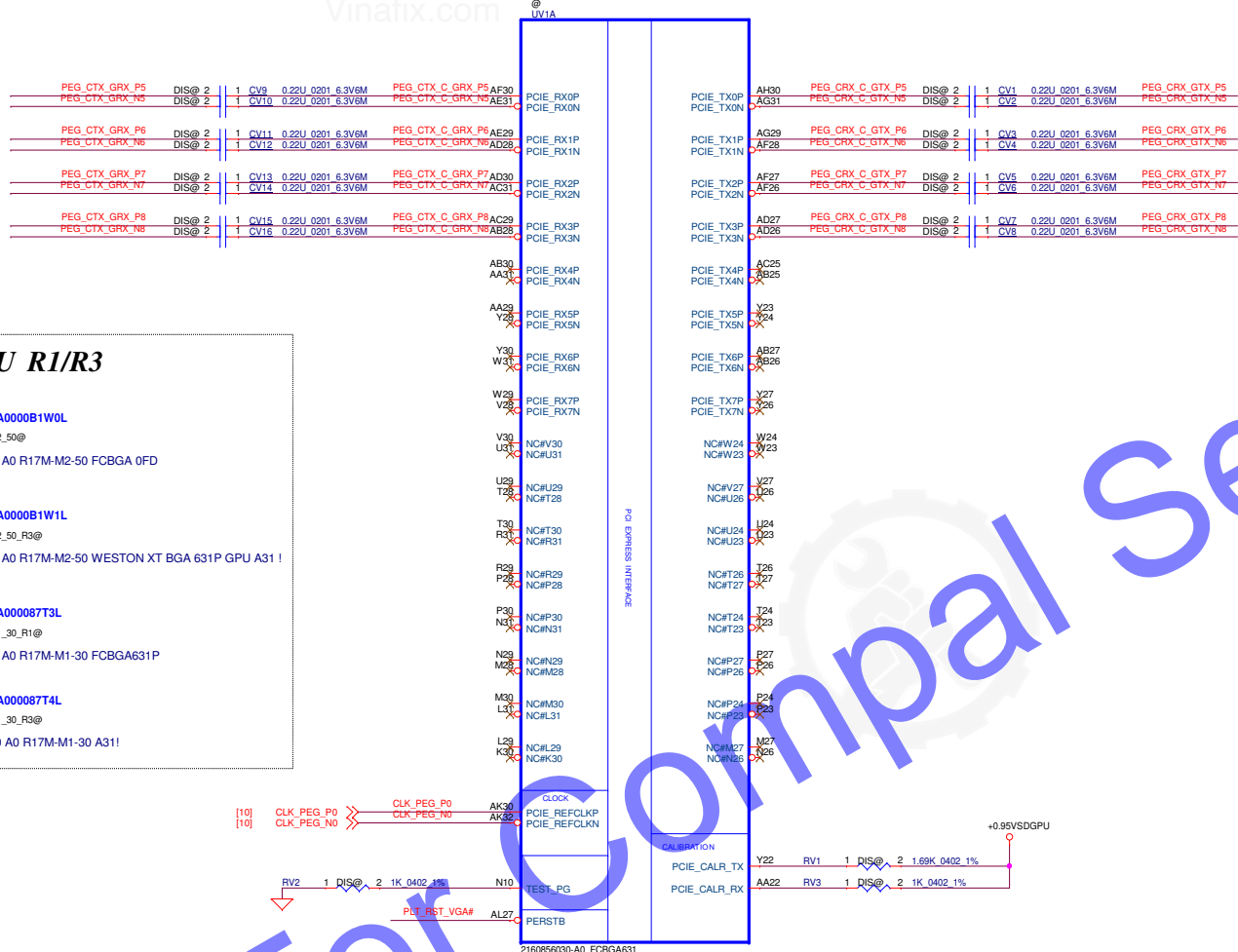
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GPU R1/R3

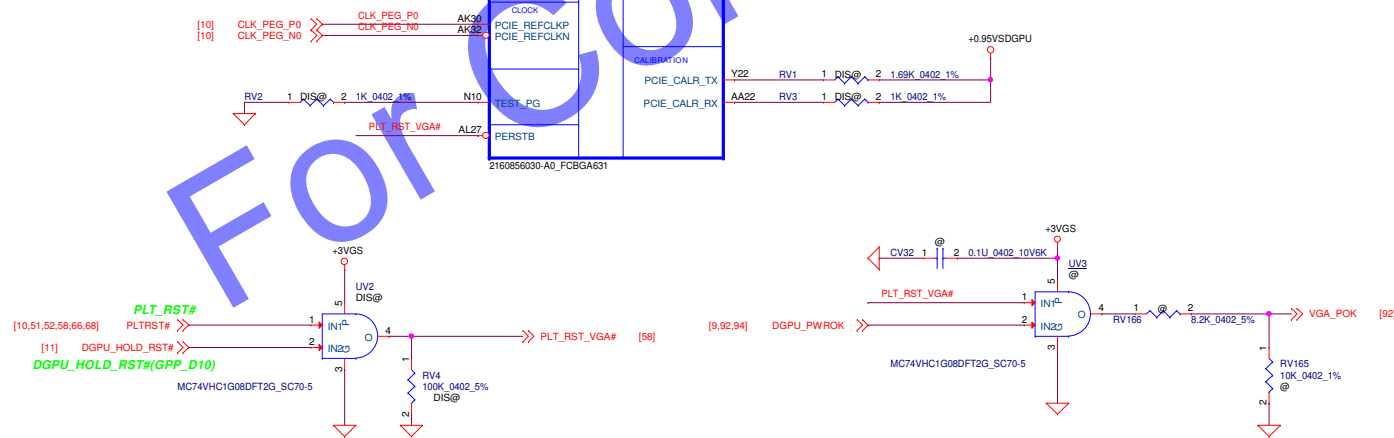
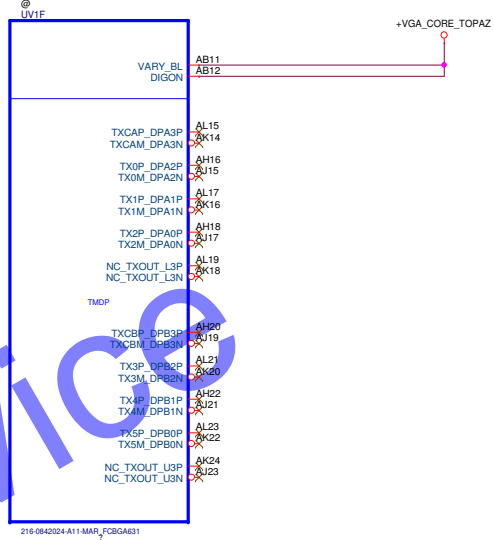
UV1 SA0000B1W0L
M2_50@
S IC 216-0889004 A0 R17M-M2-50 FCBGA 0FD

UV1 SA0000B1W1L
M2_50_R3@
S IC 216-0889004 A0 R17M-M2-50 WESTON XT BGA 631P GPU A31 !

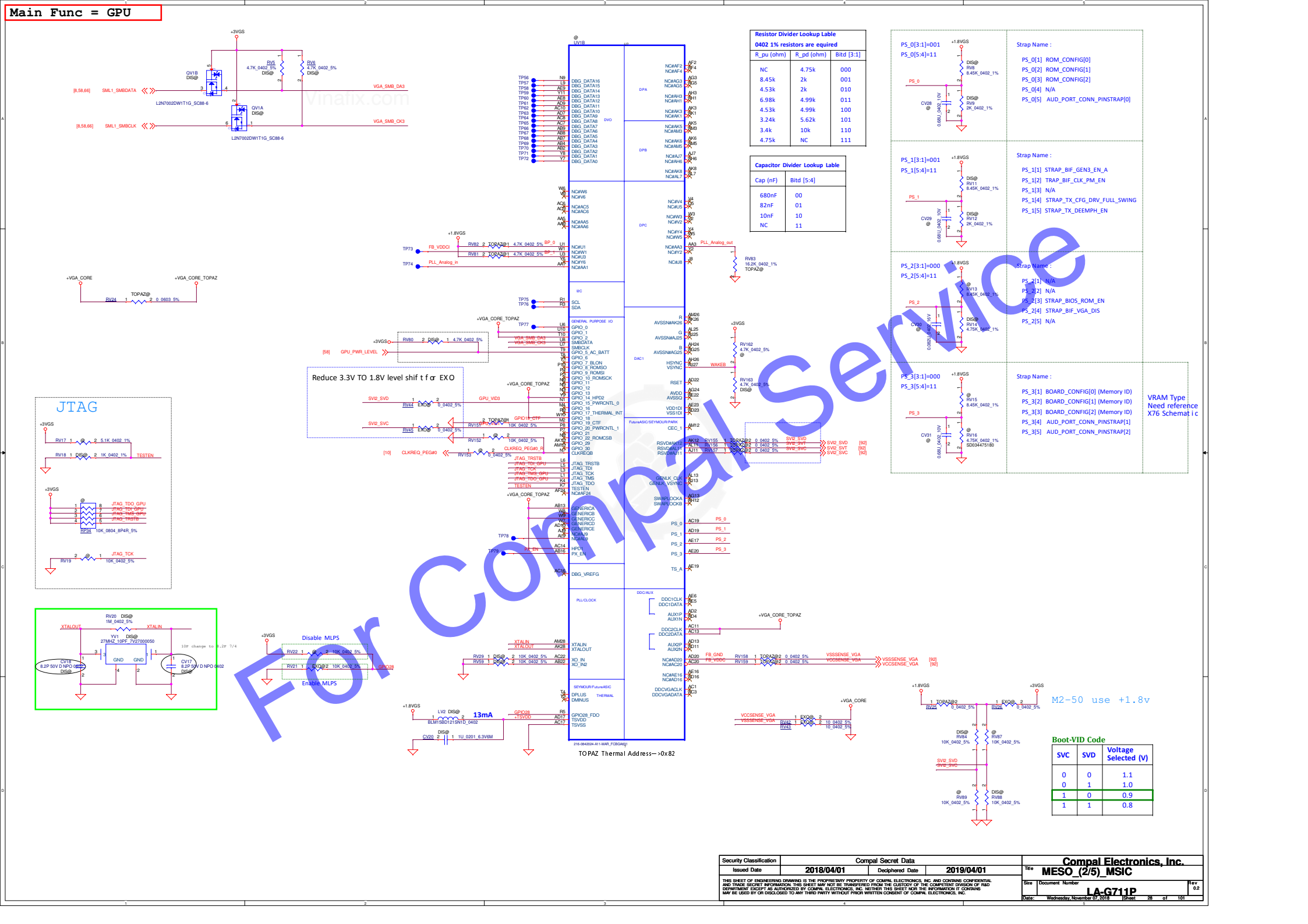
UV1 SA000087T3L
M1_30_R1@
S IC 216-0890010 A0 R17M-M1-30 FCBGA631P

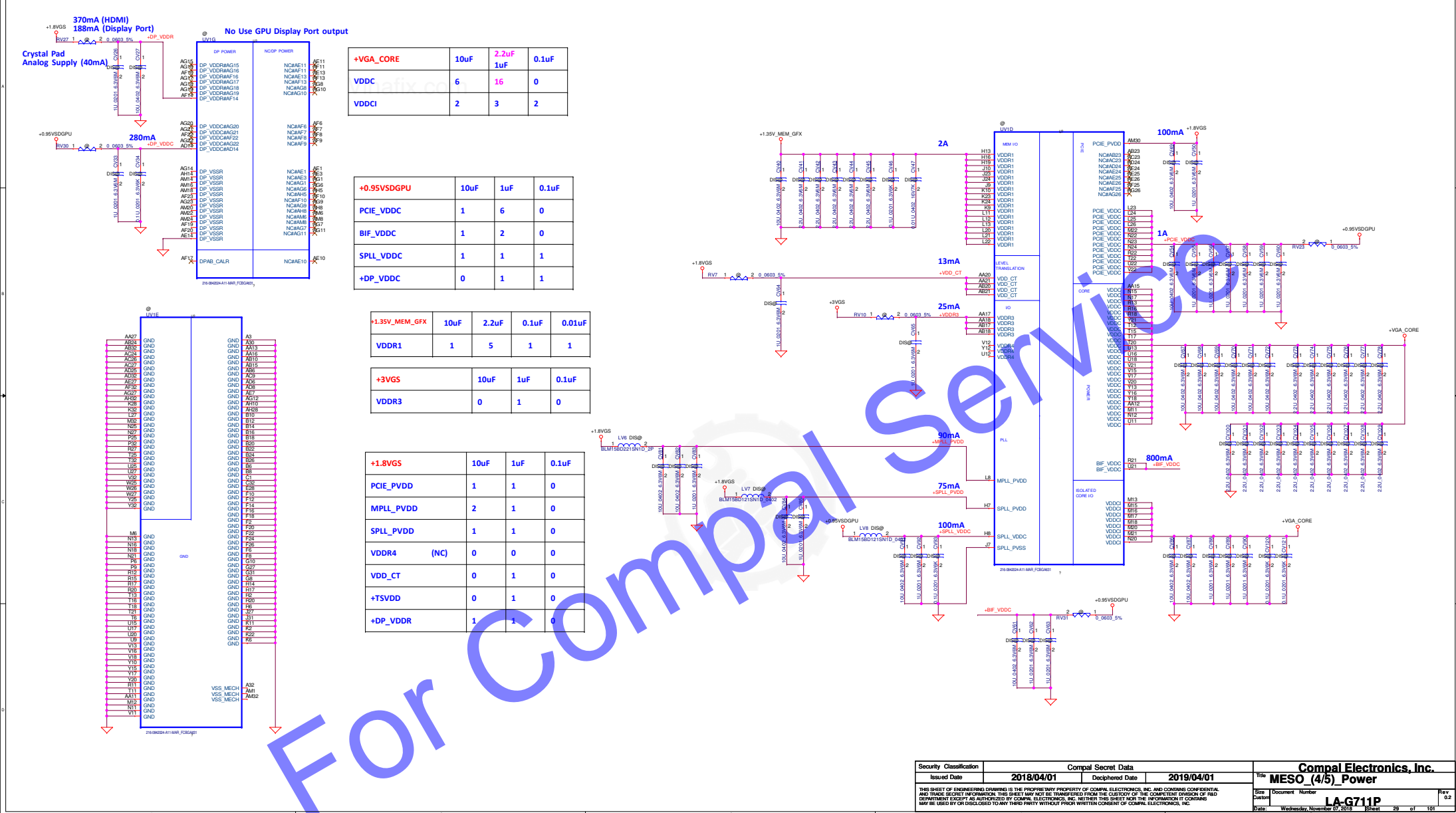
UV1 SA000087T4L
M1_30_R3@
S IC 216-0890010 A0 R17M-M1-30 A31!

No Use GPU Display Port output



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- Power-Up/Down Sequence**
1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
 2. It is recommended that the 3.3-V rail ramp up first.
 3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
 4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slow rate requirement (such as 20 mV/ μ s).
 5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
 6. For power down, reversing the ramp-up sequence is recommended.

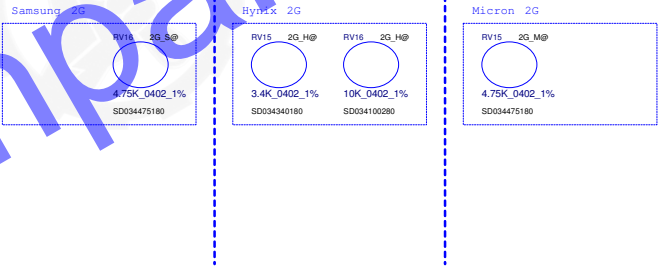
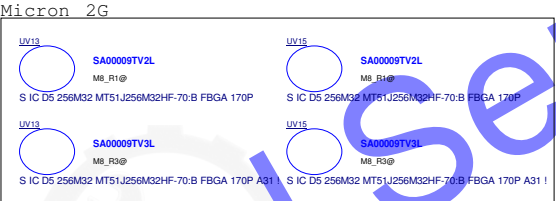
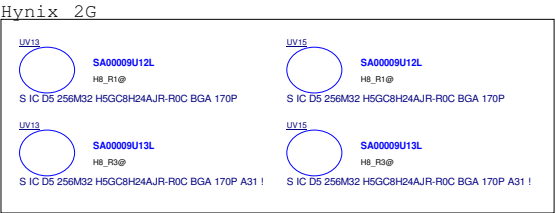
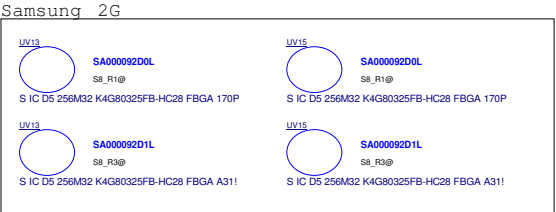
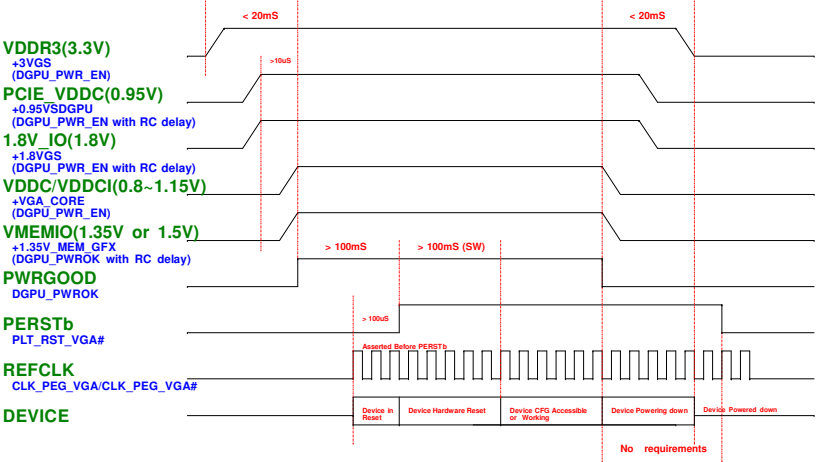


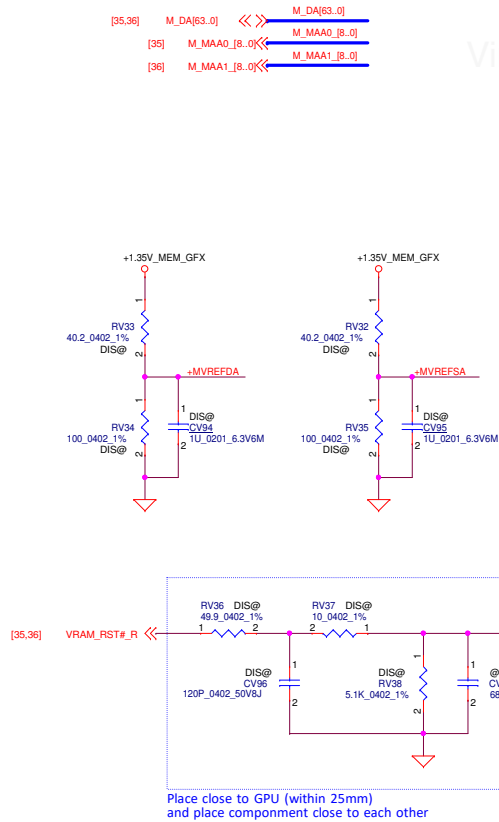
Table 3-21 Resistor Divider Lookup T.

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

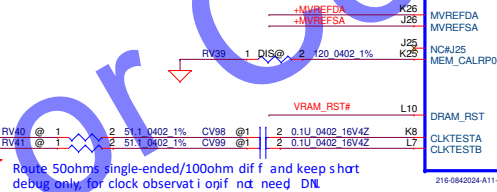
Note: 0402 1% resistors are required.

For AMD R17M-M1-30 VRAM

Memory ID	8Gb R3 P/N	Vendor	Configuration	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	2GB
110	SA00009U13L	Hynix	S IC D5 256M32 H5GC8H24AJR-ROC BGA 170P A31 !	2GB
111	SA00009TV3L	Micron	S IC D5 256M32 MT51J256M32HF-70:B FBGA 170P A31 !	2GB



Place close to GPU (within 25mm)
and place component close to each other



Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation if not need DNL

DIP		UP	
D000D0R3		D000D0R3	
M_DA0	K27	D00A_0	M_MAA0_0
M_DA1	J93	MAA0_0/MAA_0	K17
M_DA2	H30	MAA0_1/MAA_1	H23
M_DA3	H32	MAA0_2/MAA_2	G23
M_DA4	H34	MAA0_3/MAA_3	G24
M_DA5	F28	MAA0_4/MAA_4	H24
M_DA6	F29	MAA0_5/MAA_5	J19
M_DA7	G30	MAA0_6/MAA_6	K19
M_DA8	Q30	MAA0_7/MAA_7	G20
M_DA9	F27	MAA0_8/MAA_8	L17
M_DA10	A28	MAA0_9/MAA_9	L17
M_DA11	C27	MAA0_10/MAA_10	G14
M_DA12	E27	MAA1_0/MAA_8	K14
M_DA13	G26	MAA1_1/MAA_9	J11
M_DA14	D20	MAA1_2/MAA_10	H11
M_DA15	F26	MAA1_3/MAA_11	H11
M_DA16	A25	MAA1_4/MAA_12	H11
M_DA17	D20	MAA1_5/MAA_13	G11
M_DA18	E26	MAA1_6/MAA_14	L15
M_DA19	D24	MAA1_7/MAA_15	L15
M_DA20	E23	MAA1_8/MAA_16	G14
M_DA21	F25	MAA1_9/MAA_17	K6
M_DA22	D22	MAA1_10/MAA_18	E32
M_DA23	F21	MAA1_11/MAA_19	E30
M_DA24	D20	MAA1_12/MAA_20	A21
M_DA25	D20	MAA1_13/MAA_21	E11
M_DA26	E19	MAA1_14/MAA_22	E13
M_DA27	A19	MAA1_15/MAA_23	D13
M_DA28	D20	MAA1_16/MAA_24	F4
M_DA29	F19	MAA1_17/MAA_25	H28
M_DA30	A17	MAA1_18/MAA_26	C27
M_DA31	C17	MAA1_19/MAA_27	A23
M_DA32	E17	MAA1_20/MAA_28	E19
M_DA33	D16	MAA1_21/MAA_29	E16
M_DA34	F15	MAA1_22/MAA_30	D10
M_DA35	A15	MAA1_23/MAA_31	G5
M_DA36	D14	MAA1_24/MAA_32	D6
M_DA37	F13	MAA1_25/MAA_33	H27
M_DA38	A13	MAA1_26/MAA_34	C27
M_DA39	C13	MAA1_27/MAA_35	A23
M_DA40	E11	MAA1_28/MAA_36	E19
M_DA41	A11	MAA1_29/MAA_37	E16
M_DA42	C11	MAA1_30/MAA_38	D10
M_DA43	F11	MAA1_31/MAA_39	G5
M_DA44	D9	MAA1_32/MAA_40	D6
M_DA45	C9	MAA1_33/MAA_41	H28
M_DA46	F9	MAA1_34/MAA_42	C27
M_DA47	A9	MAA1_35/MAA_43	A23
M_DA48	D8	MAA1_36/MAA_44	E19
M_DA49	E7	MAA1_37/MAA_45	E16
M_DA50	A7	MAA1_38/MAA_46	D10
M_DA51	C7	MAA1_39/MAA_47	G5
M_DA52	A7	MAA1_40/MAA_48	D6
M_DA53	E5	MAA1_41/MAA_49	H27
M_DA54	C5	MAA1_42/MAA_50	C27
M_DA55	E5	MAA1_43/MAA_51	A23
M_DA56	C5	MAA1_44/MAA_52	E19
M_DA57	A5	MAA1_45/MAA_53	E16
M_DA58	C5	MAA1_46/MAA_54	D10
M_DA59	A5	MAA1_47/MAA_55	G5
M_DA60	C5	MAA1_48/MAA_56	D6
M_DA61	A5	MAA1_49/MAA_57	H28
M_DA62	C5	MAA1_50/MAA_58	C27
M_DA63	A5	MAA1_51/MAA_59	A23
M_DA64	C5	MAA1_52/MAA_60	E19
M_DA65	A5	MAA1_53/MAA_61	E16
M_DA66	C5	MAA1_54/MAA_62	D10
M_DA67	A5	MAA1_55/MAA_63	G5
M_DA68	C5	MAA1_56/MAA_64	D6
M_DA69	A5	MAA1_57/MAA_65	H27
M_DA70	C5	MAA1_58/MAA_66	C27
M_DA71	A5	MAA1_59/MAA_67	A23
M_DA72	C5	MAA1_60/MAA_68	E19
M_DA73	A5	MAA1_61/MAA_69	E16
M_DA74	C5	MAA1_62/MAA_70	D10
M_DA75	A5	MAA1_63/MAA_71	G5
M_DA76	C5	MAA1_64/MAA_72	D6
M_DA77	A5	MAA1_65/MAA_73	H28
M_DA78	C5	MAA1_66/MAA_74	C27
M_DA79	A5	MAA1_67/MAA_75	A23
M_DA80	C5	MAA1_68/MAA_76	E19
M_DA81	A5	MAA1_69/MAA_77	E16
M_DA82	C5	MAA1_70/MAA_78	D10
M_DA83	A5	MAA1_71/MAA_79	G5
M_DA84	C5	MAA1_72/MAA_80	D6
M_DA85	A5	MAA1_73/MAA_81	H27
M_DA86	C5	MAA1_74/MAA_82	C27
M_DA87	A5	MAA1_75/MAA_83	A23
M_DA88	C5	MAA1_76/MAA_84	E19
M_DA89	A5	MAA1_77/MAA_85	E16

Main Function:

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				Size	Rev
				Document Number	0.2
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				Size	Rev
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Main Function:

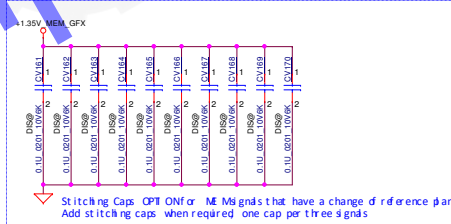
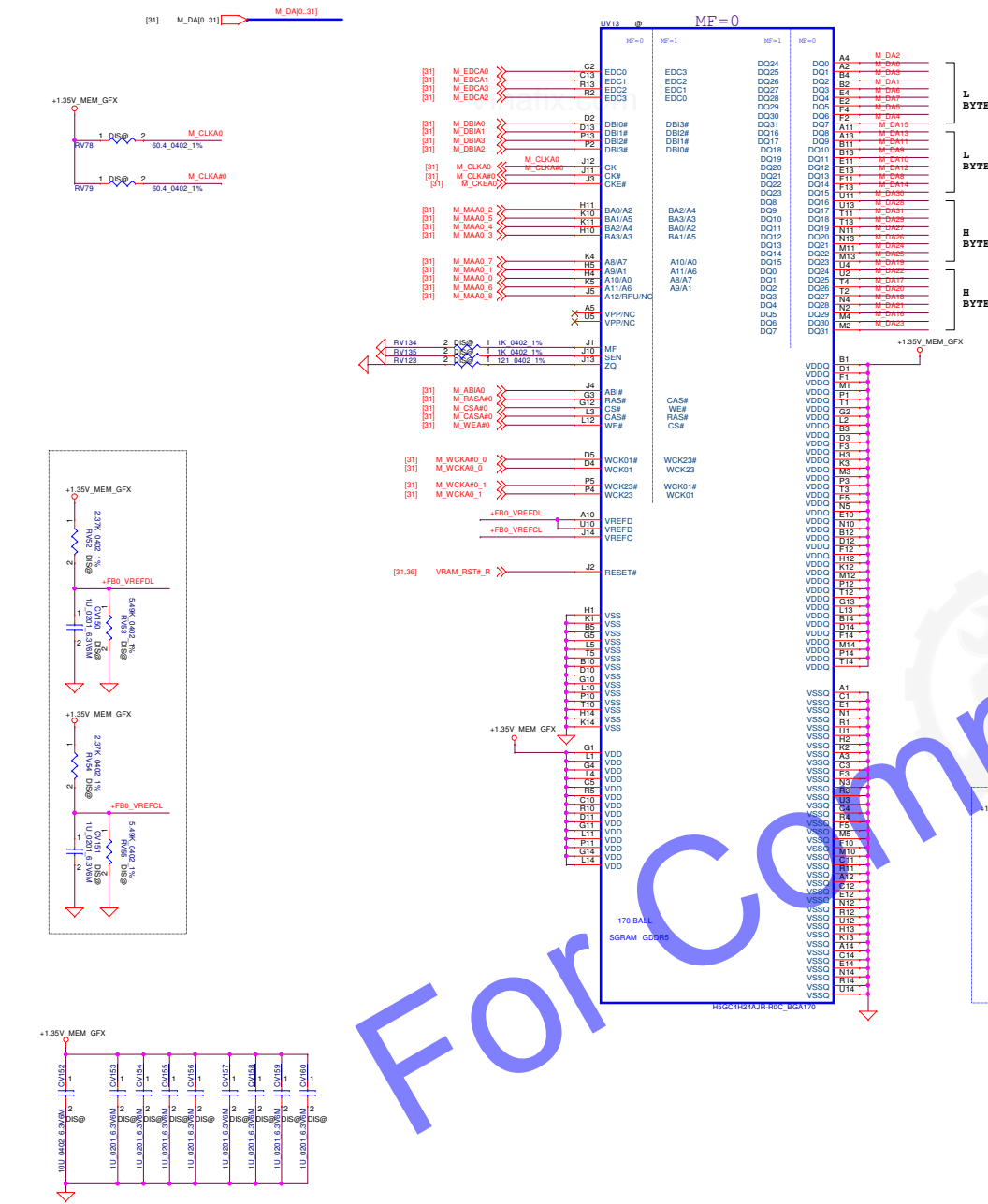
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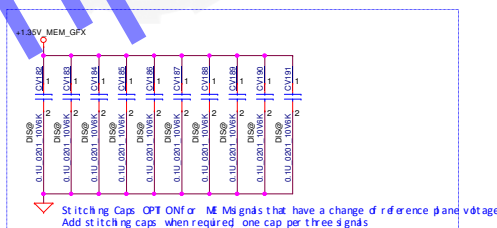
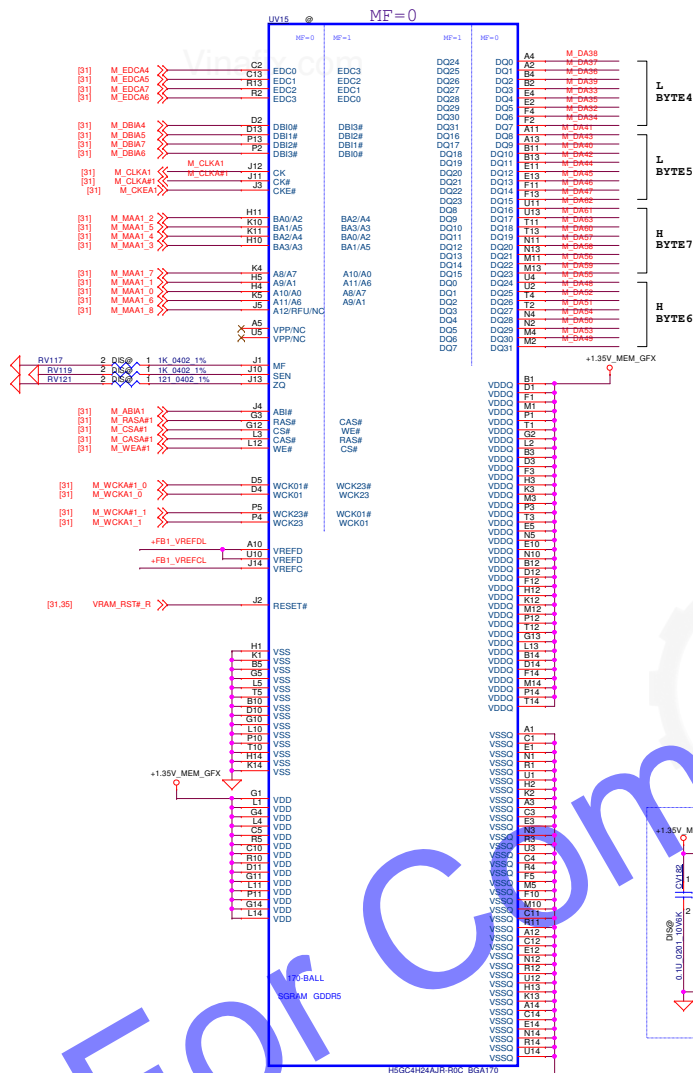
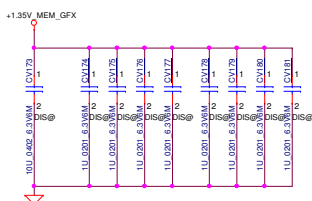
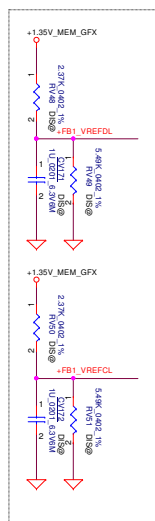
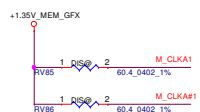
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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title	
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Main Func = GDDR5



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				MESO GDDR5 A0	
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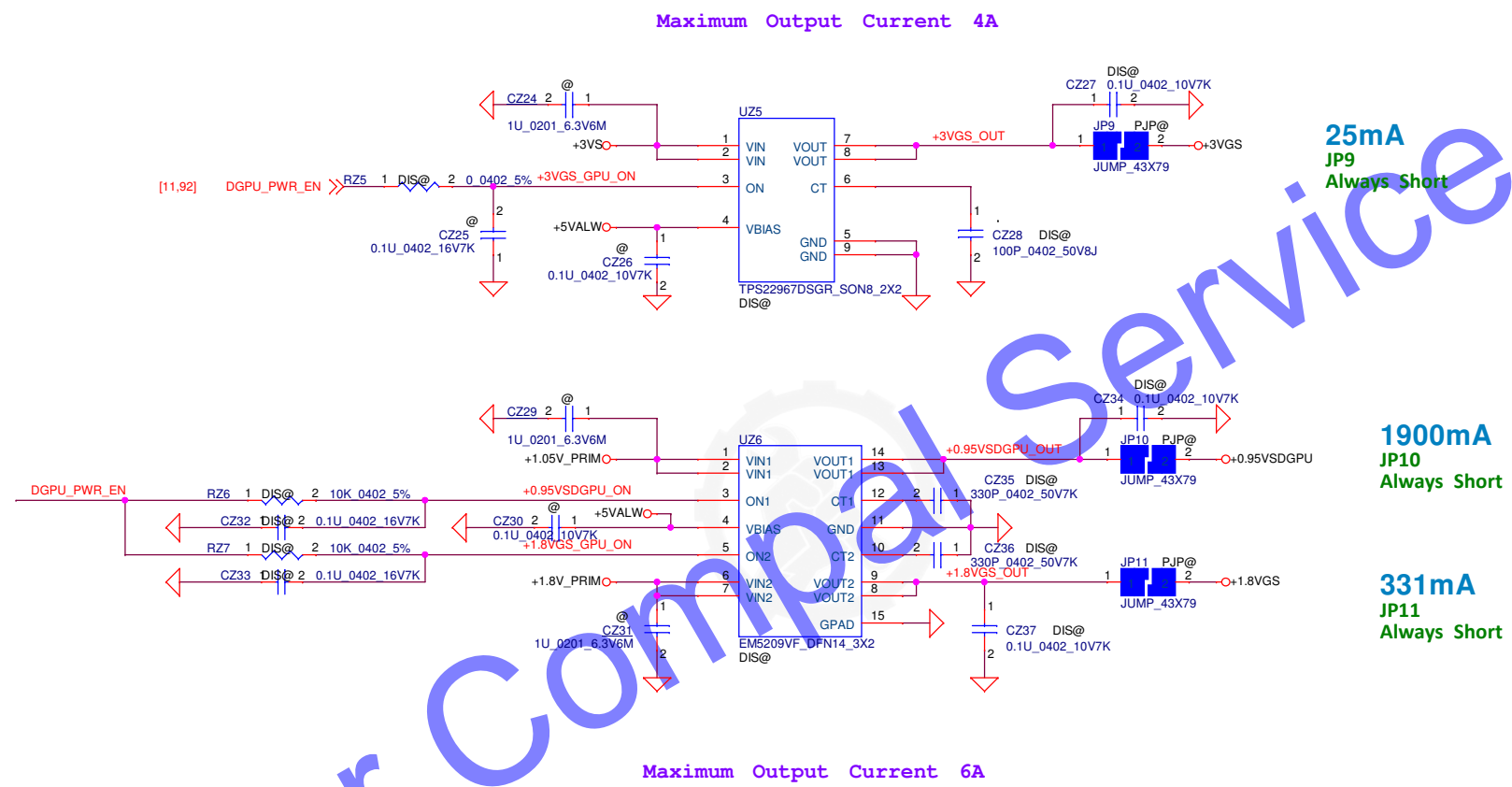
Main Func = GDDR5



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Size	Document Number	LA-67111P Date: Wednesday, November 07, 2019 12:24 PM		Rev: 0.1

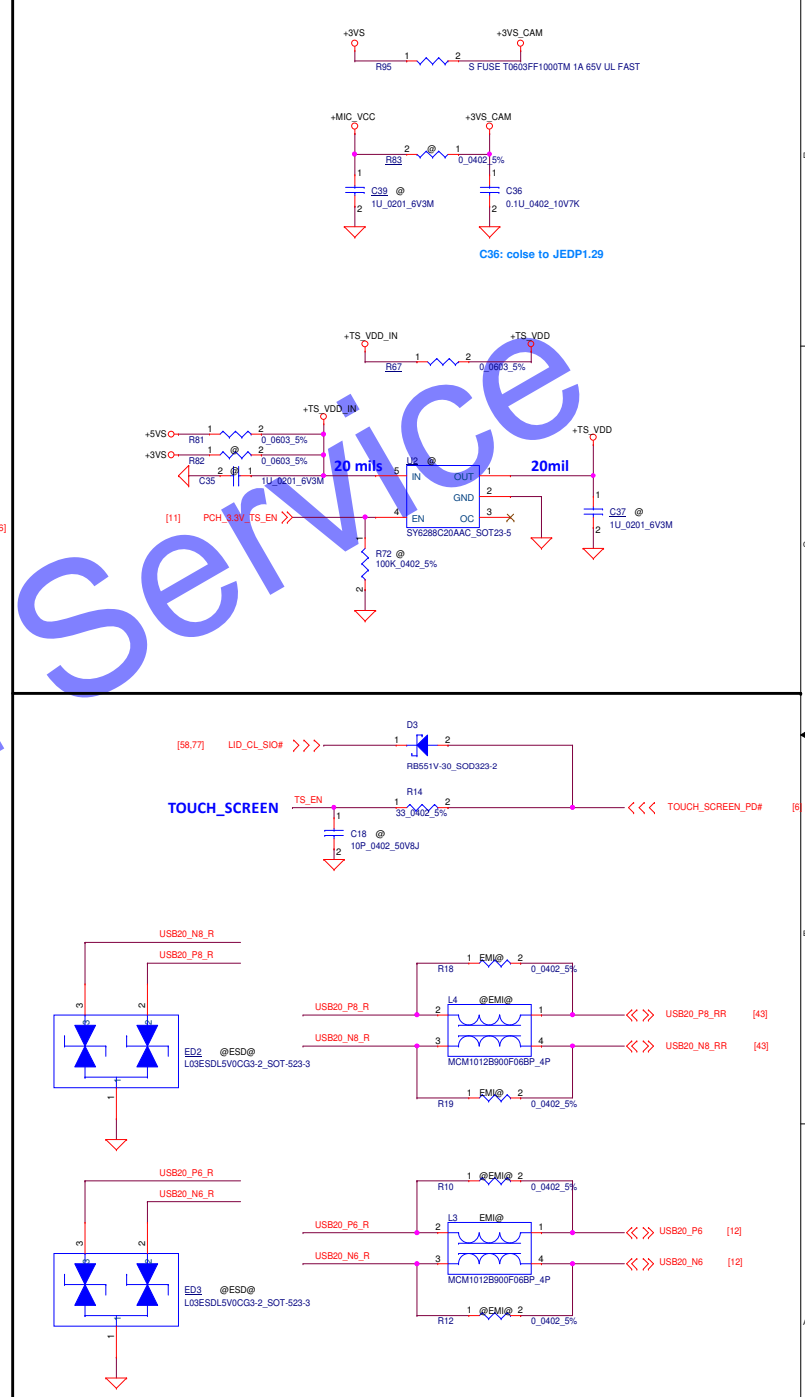
Main Func = GPU

+3V/+0.95V/+1.8V for GPU



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Main Func = CAM&MIC, TS



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					LA-G711P	0.2
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Main Function:

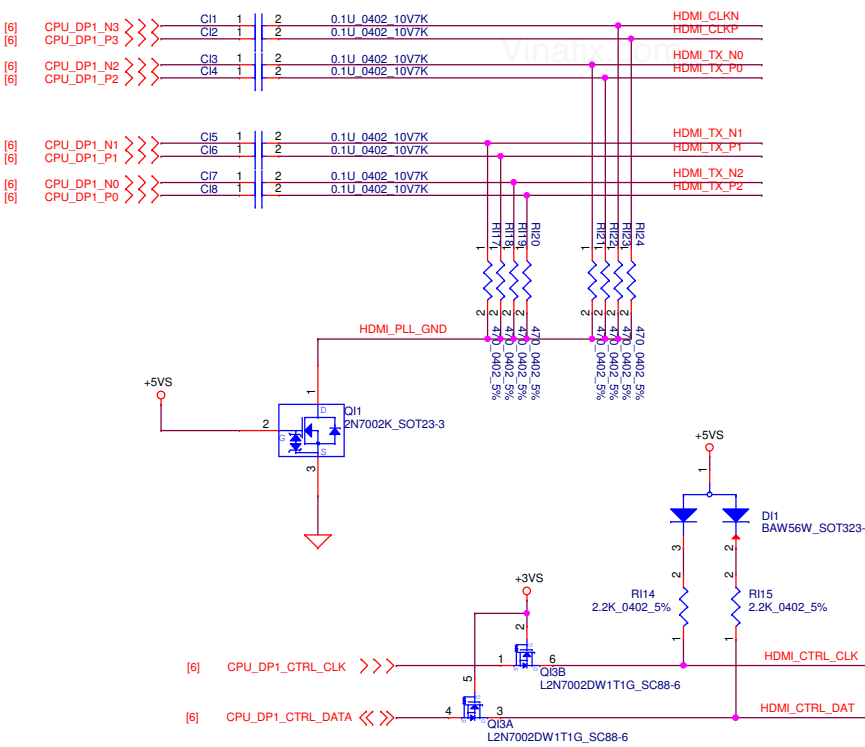
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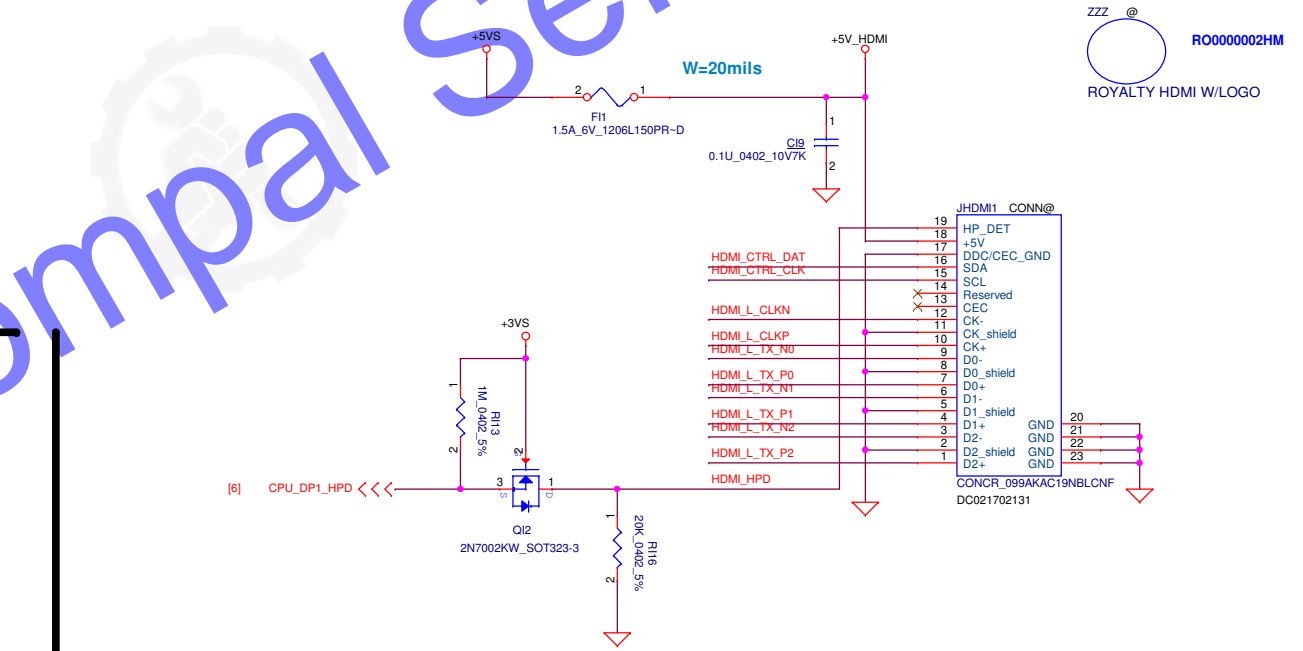
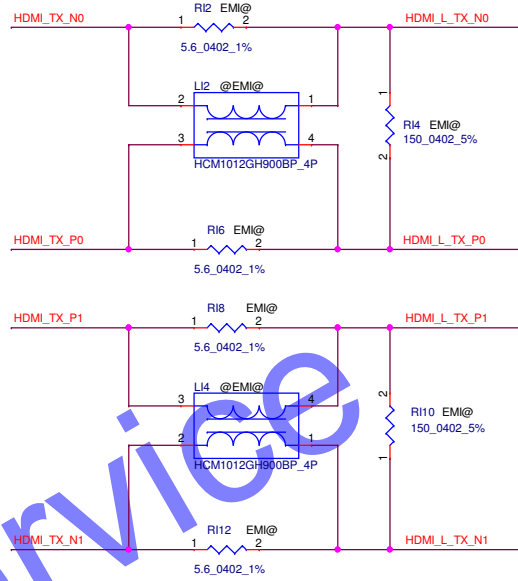
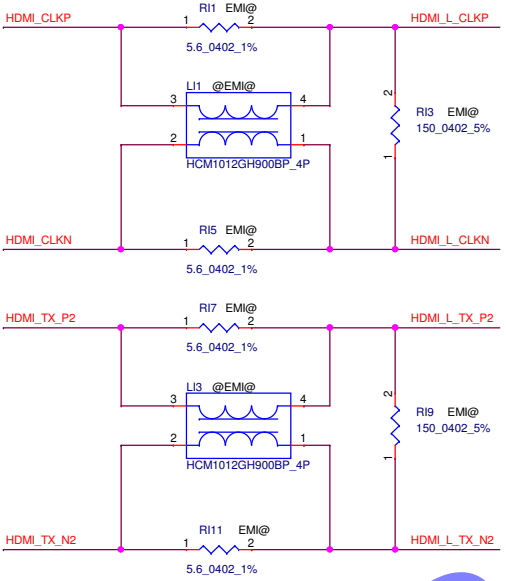
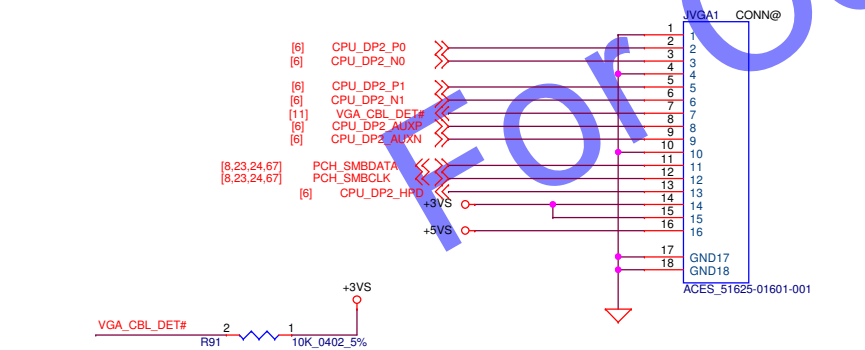
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Main Func = HDMI



Main Func = VGA



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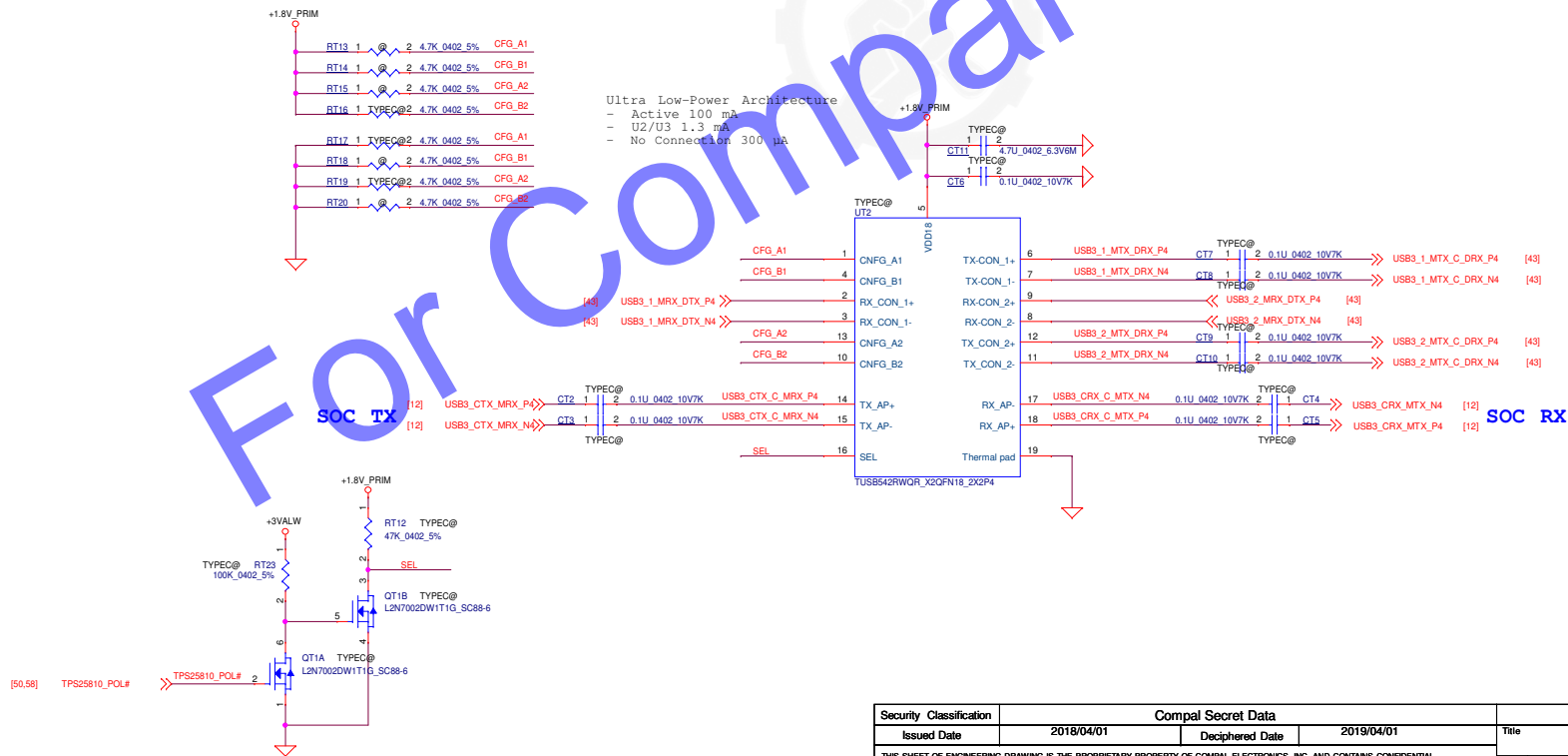
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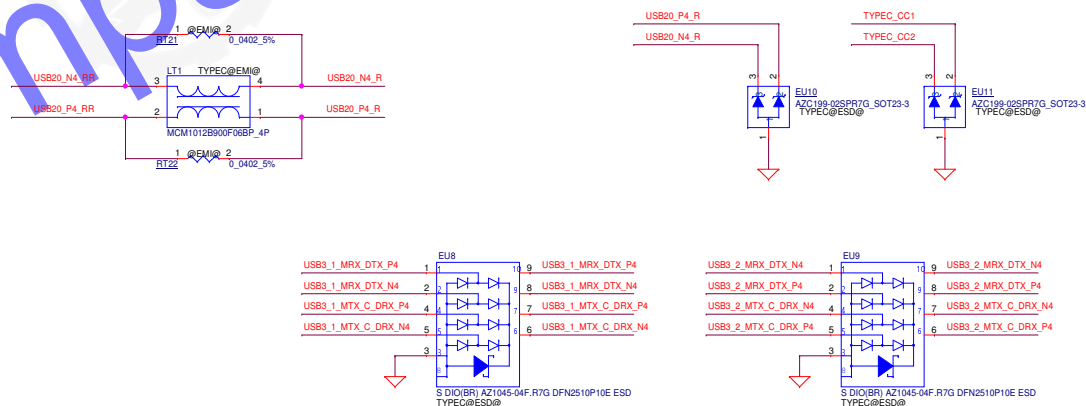
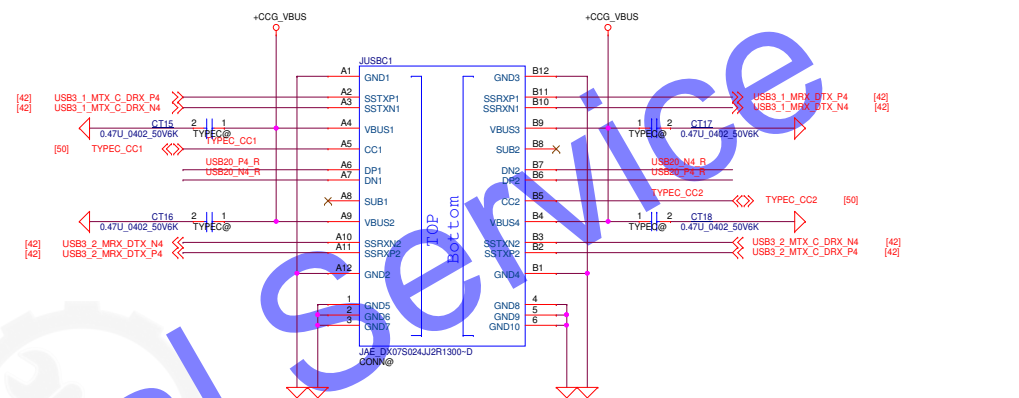
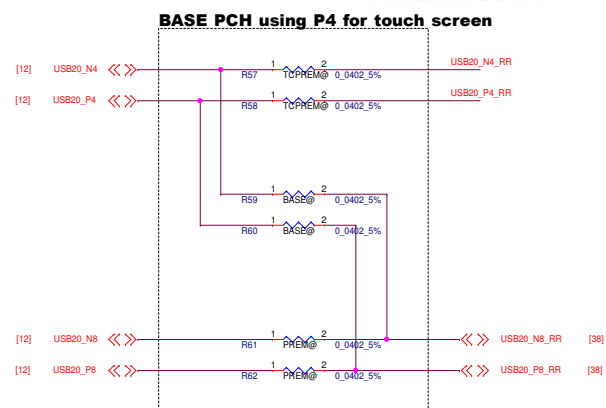
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Main Func = Typec MUX



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					<i>LA-G711P</i>	02
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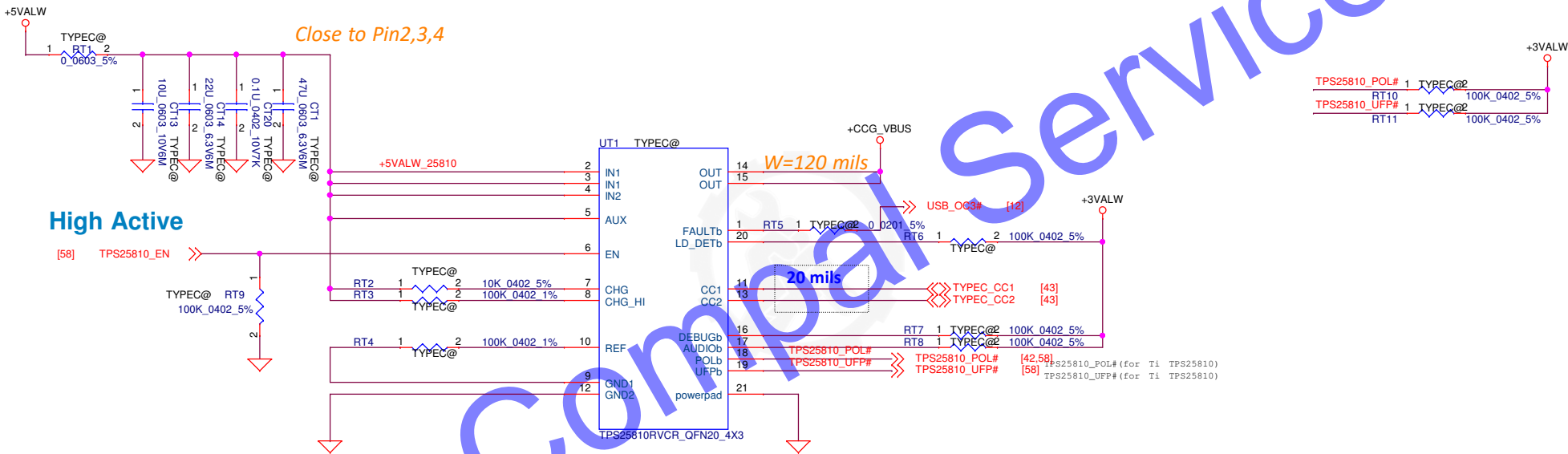
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Main Function: TYPE-C_Power Path

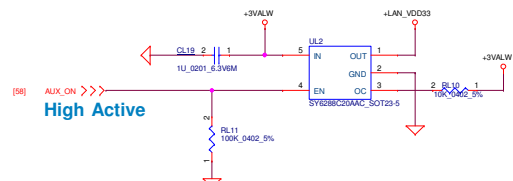
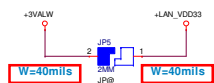
Main Func = Power Switch

5V@3A



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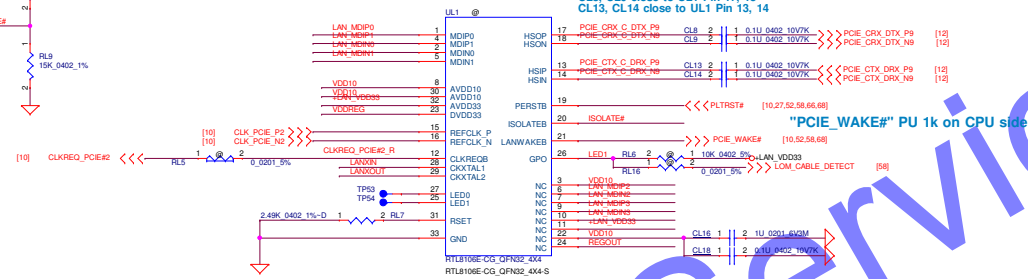
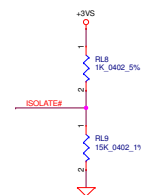
Main Func = LAN



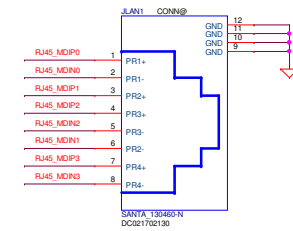
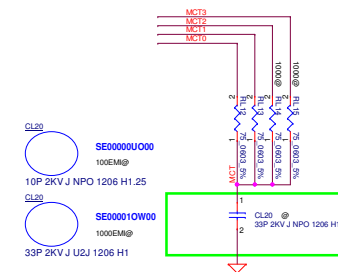
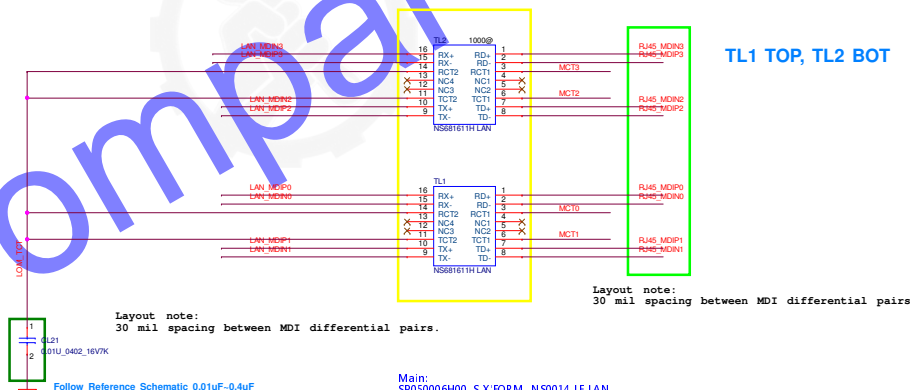
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RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

LAN CHIP 10/100/1000

RTL8111N-CG	RTL8106E-CG
SA000080P00	SA000045Y00
LD0 mode	LD0 mode
10/100/1000M	10/100M

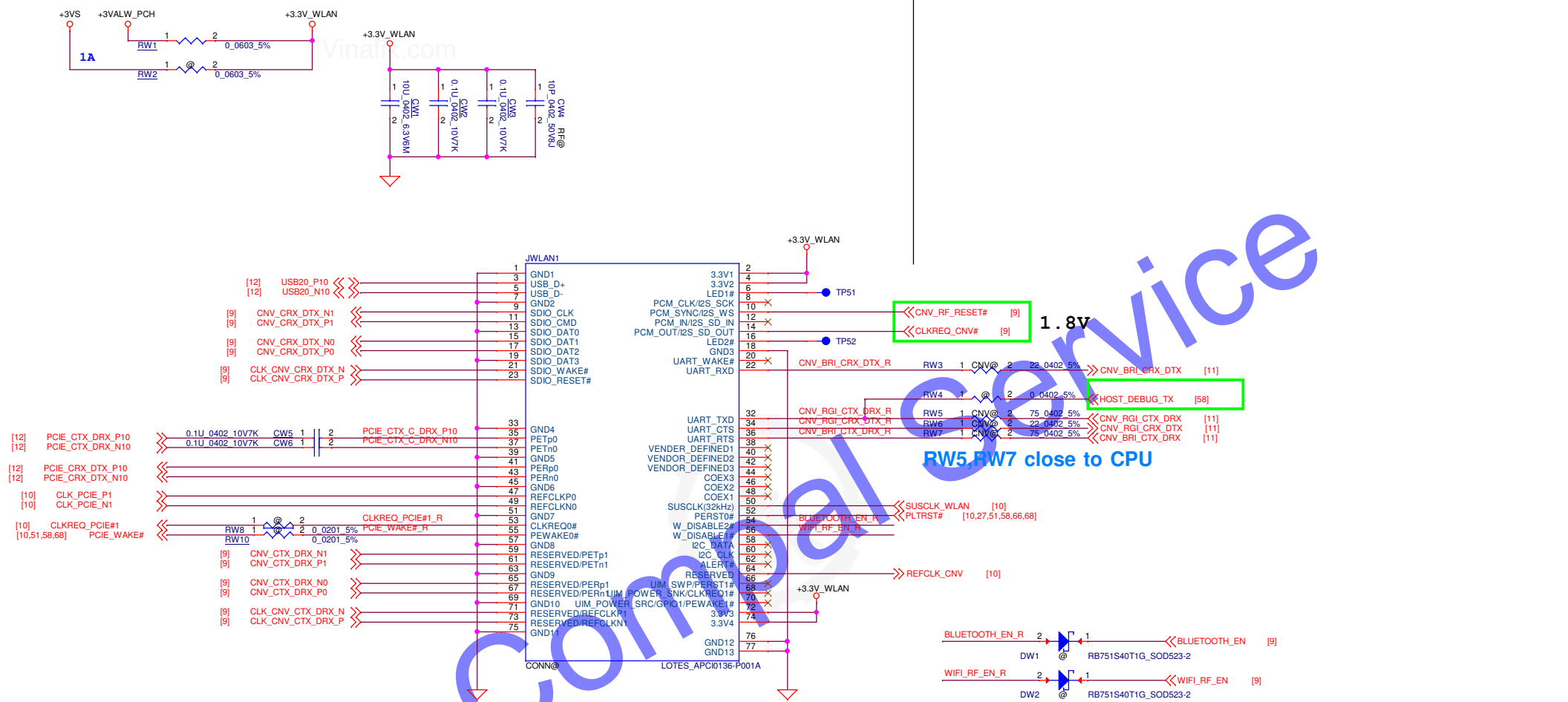


Main Func = LAN LAN TransFormer 10/100M x2



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Main Func = WLAN E Key CONN



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Main Function: WIGIG / WIDI

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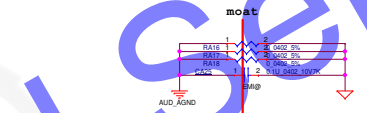
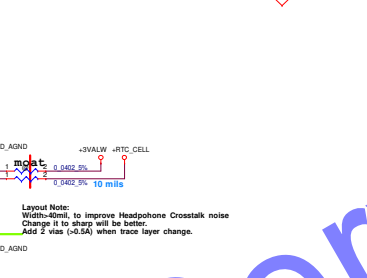
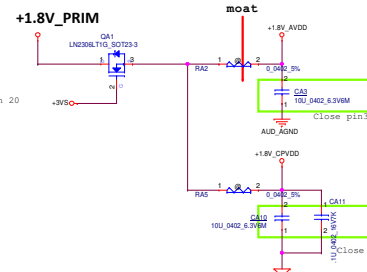
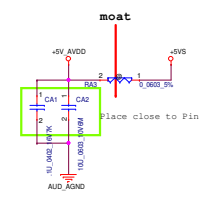
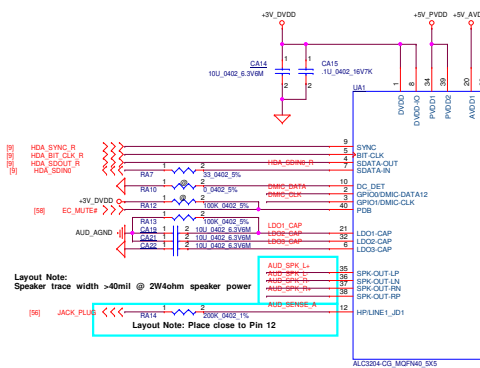
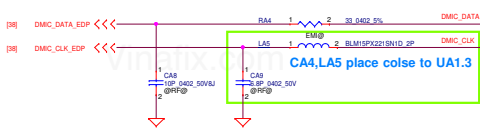
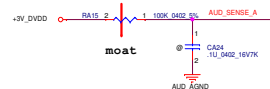
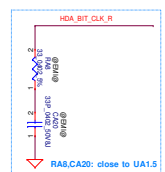
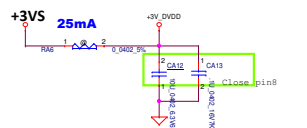
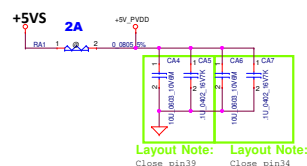
Main Function:

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				LA-G711P	
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Main Func = Audio

Jack

Audio

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CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

SPK_R

SPK_R

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				Size	Rev
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Main Function:

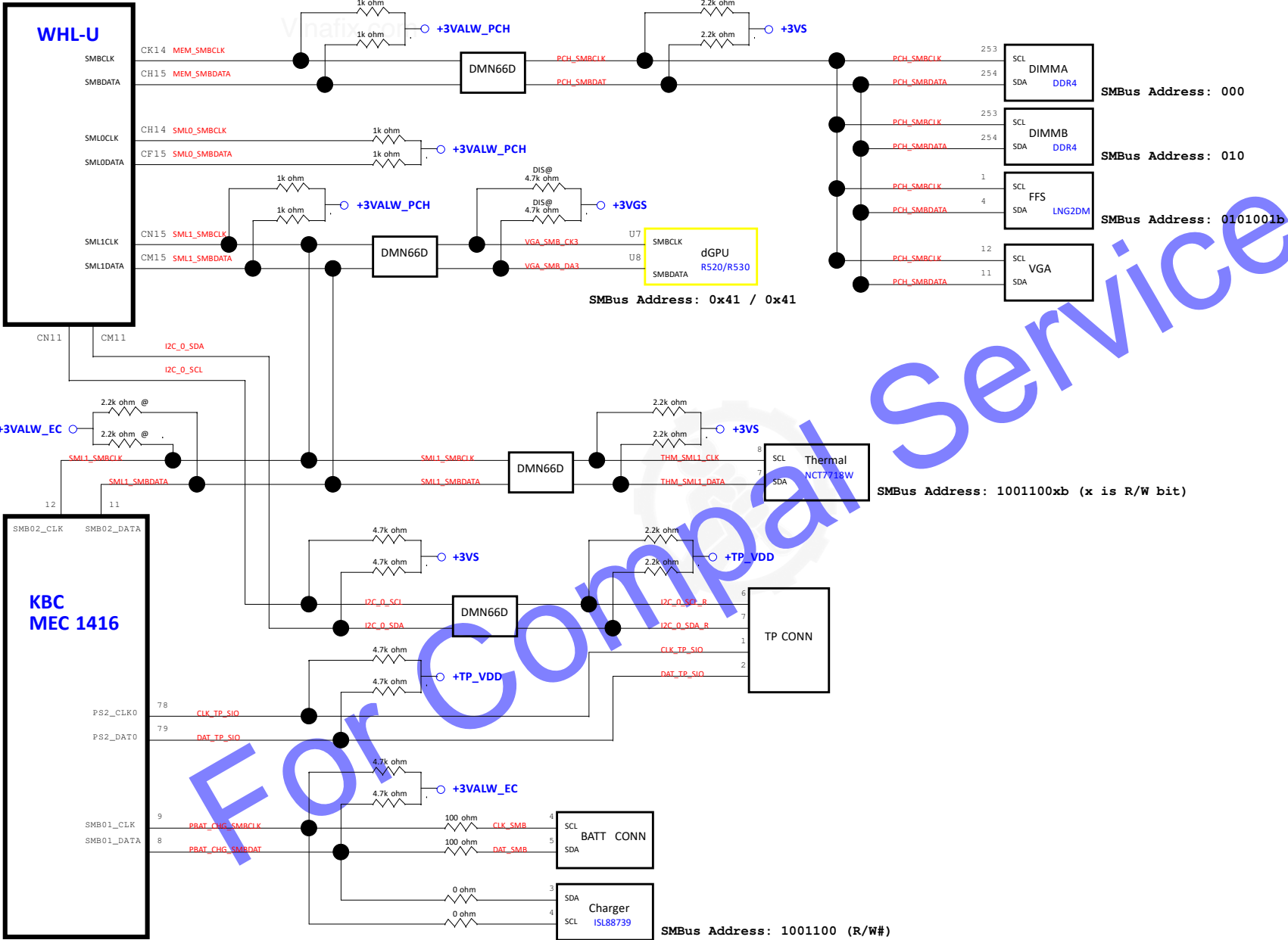
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				Document Number	0.2
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Main Function:SMB/I2C Block Diagrams



Main Function:

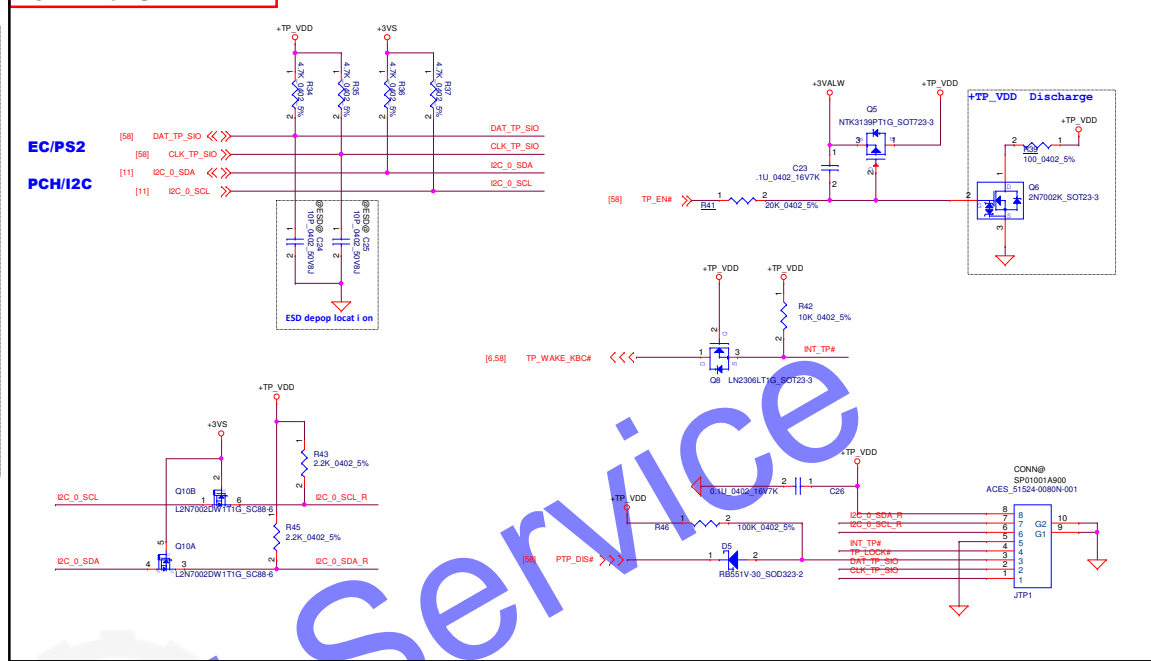
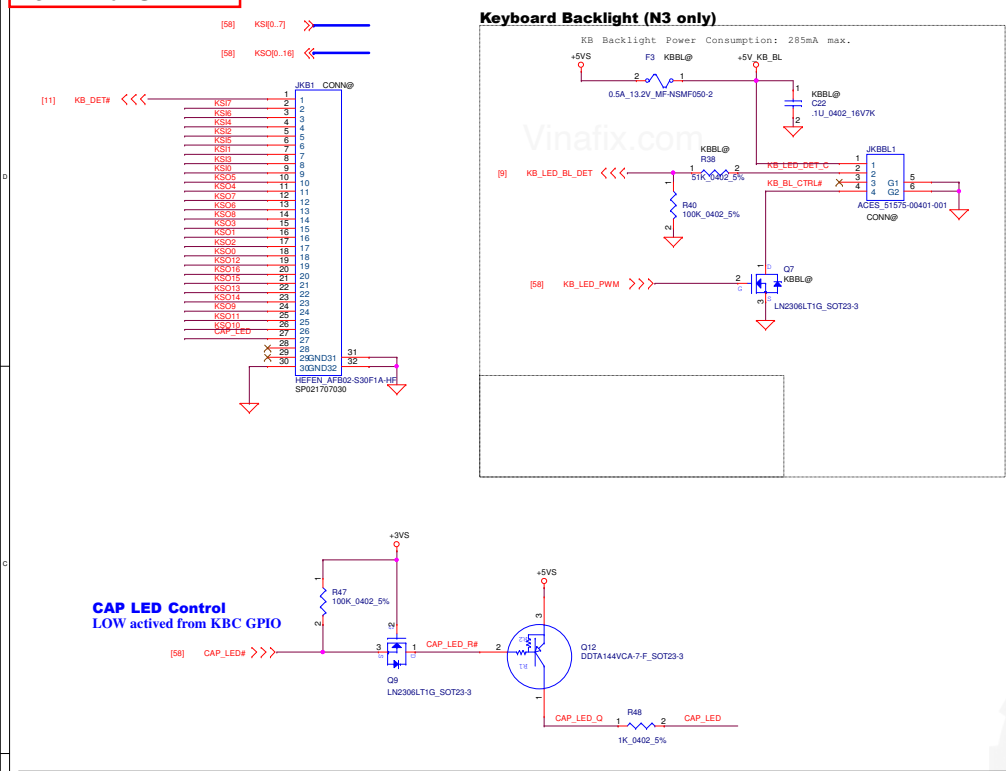
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				Size	Rev
				Document Number	0.2
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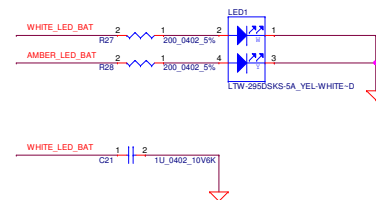
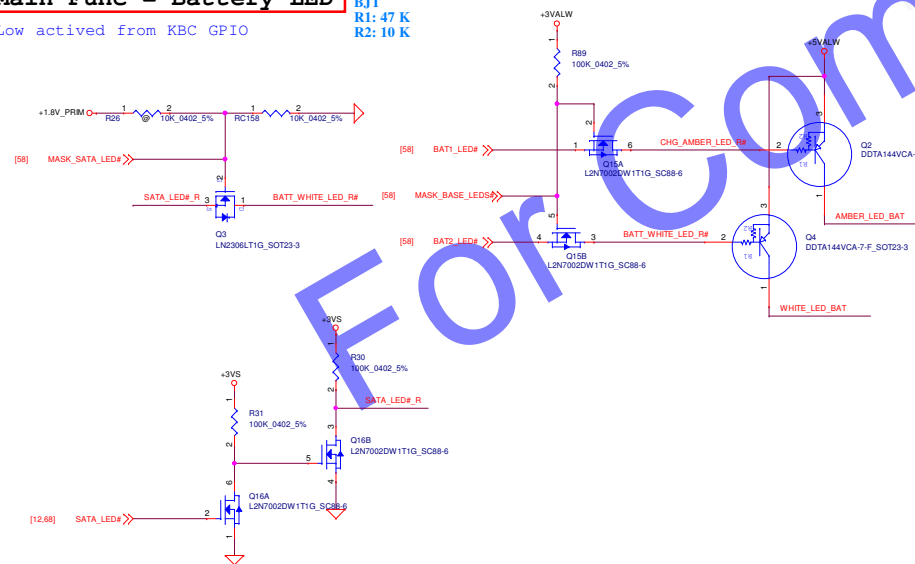
3
Main Func = TPAD



Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



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Main Function:

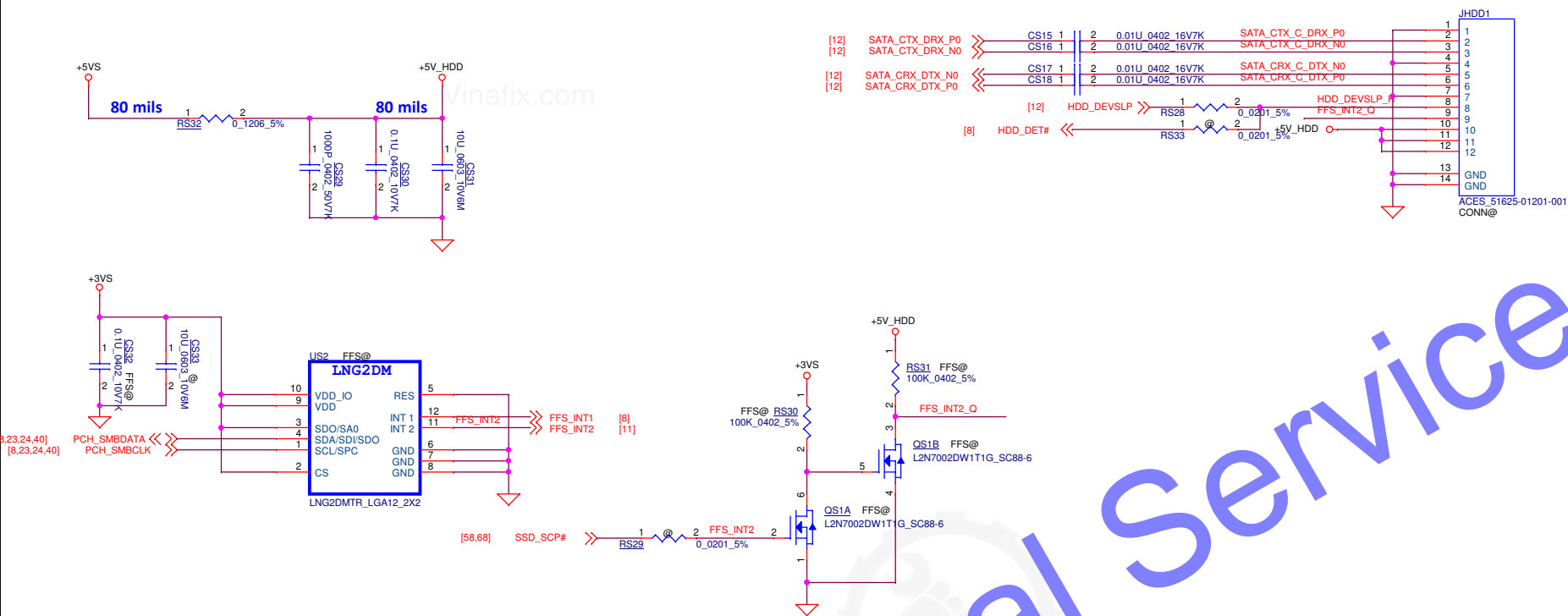
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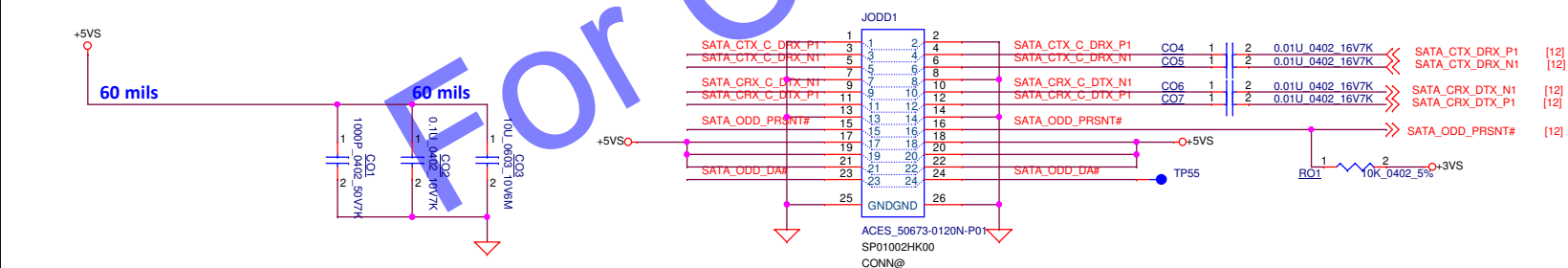
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Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	8
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	9

Main Func = ODD

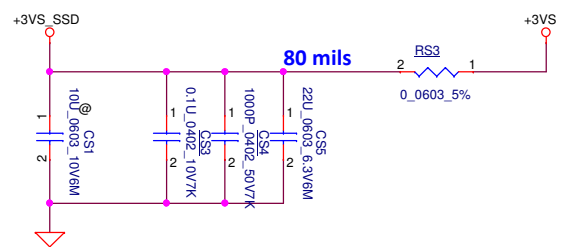


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSENT	P1	8
5V	P2	9
5V	P3	10
Attention	P4	12
GND	P5	
GND	P6	

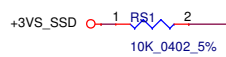
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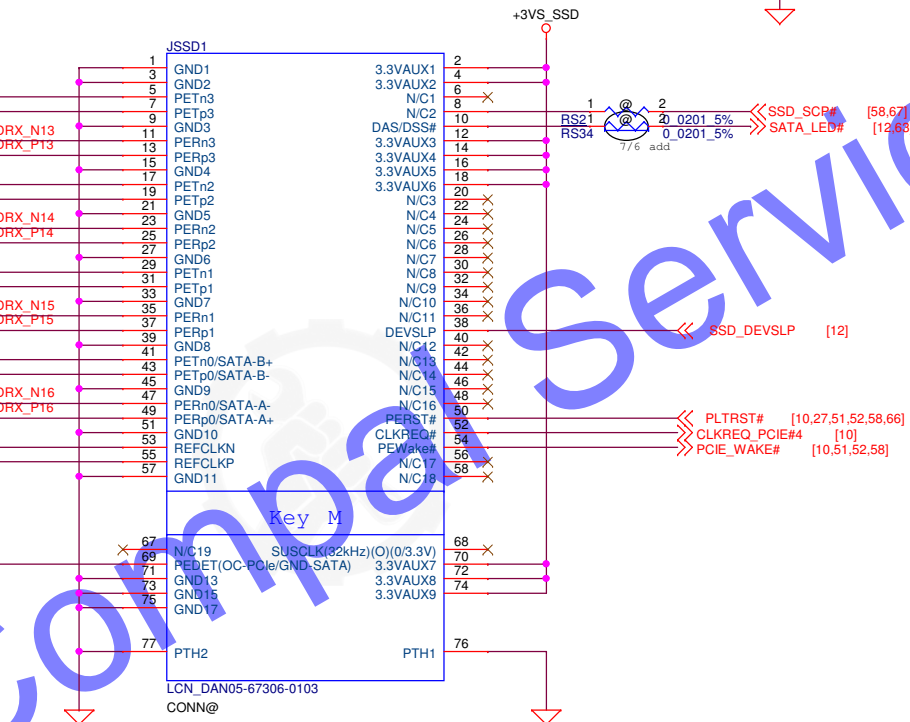
NGFF Key M



- [12] PCIE_CRX_DTX_N13
- [12] PCIE_CRX_DTX_P13
- [12] PCIE_CTX_DRX_N13
- [12] PCIE_CTX_DRX_P13
- [12] PCIE_CRX_DTX_N14
- [12] PCIE_CRX_DTX_P14
- [12] PCIE_CTX_DRX_N14
- [12] PCIE_CTX_DRX_P14
- [12] PCIE_CRX_DTX_N15
- [12] PCIE_CRX_DTX_P15
- [12] PCIE_CTX_DRX_N15
- [12] PCIE_CTX_DRX_P15
- [12] PCIE_CRX_DTX_N16
- [12] PCIE_CRX_DTX_P16
- [12] PCIE_CTX_DRX_N16
- [12] PCIE_CTX_DRX_P16



PEDET	Module Type
0	SATA
1	PCIE



Main Func = eMMC

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Main Function:

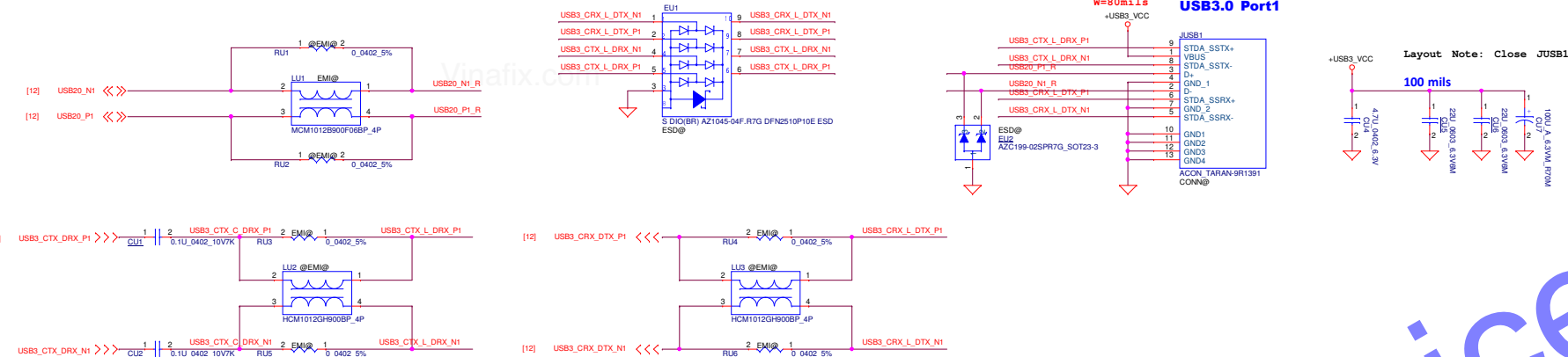
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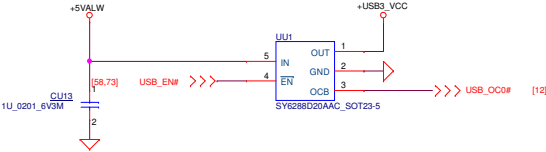
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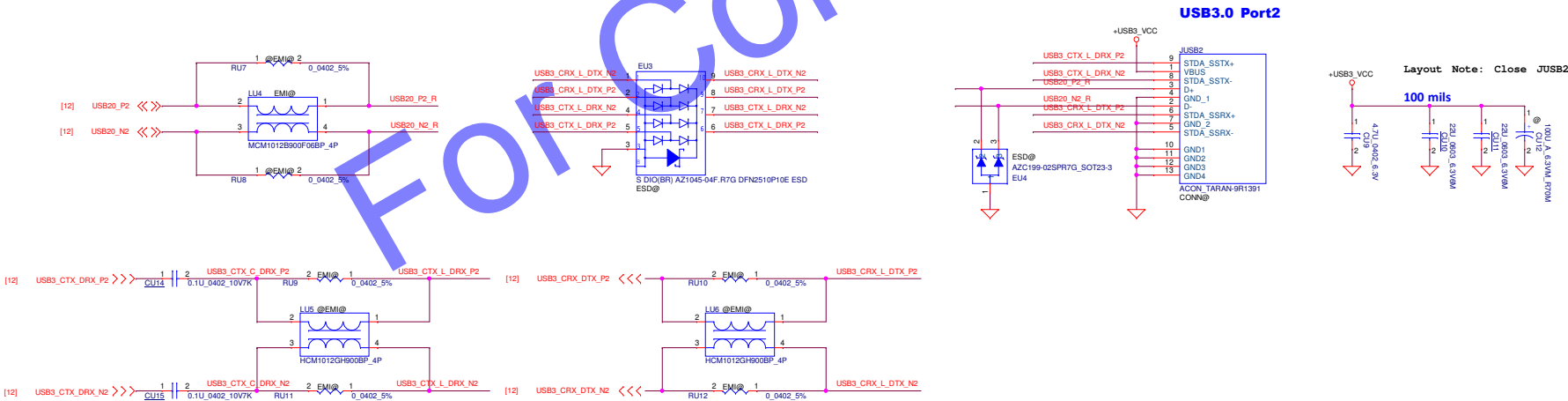
Main Func = USB3.0 Port1



Maximum Output
Current
2A



Main Func = USB3.0 Port2



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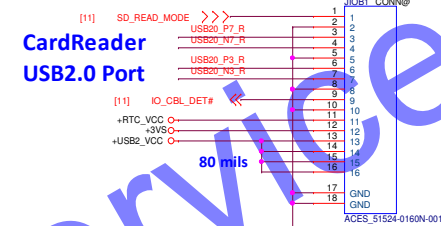
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Main Func = USB2.0 Port3 + Card Reader on IO/B



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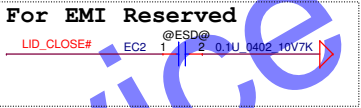
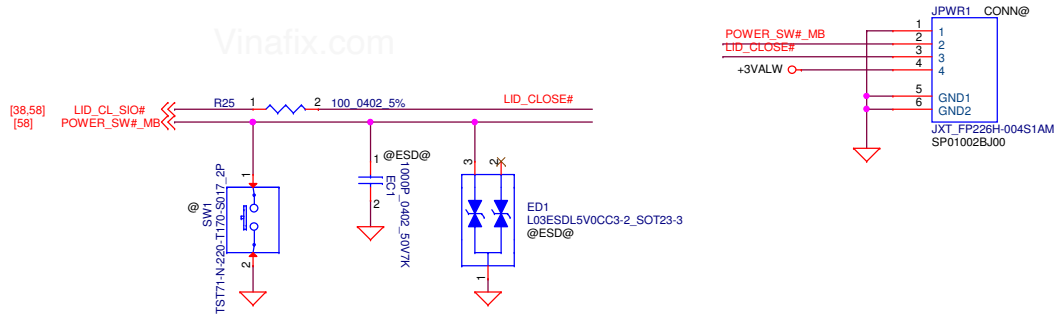
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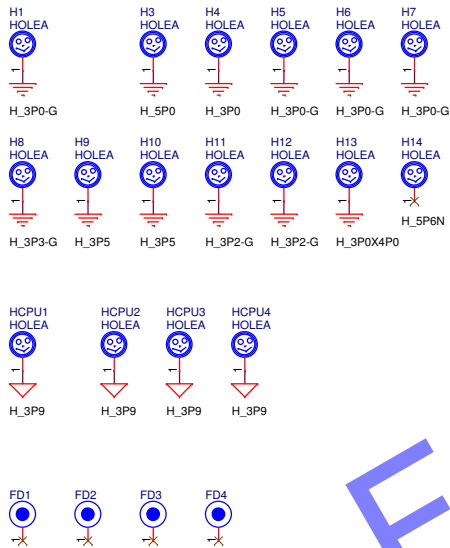
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Main Func = Power BTN

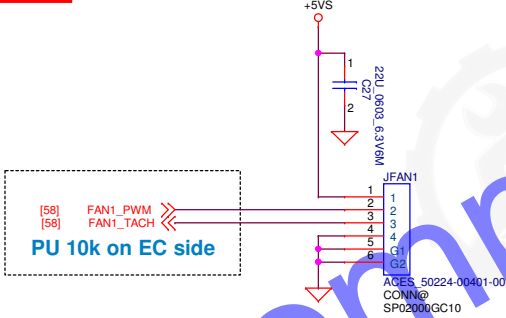
Low actived from KBC GPIO



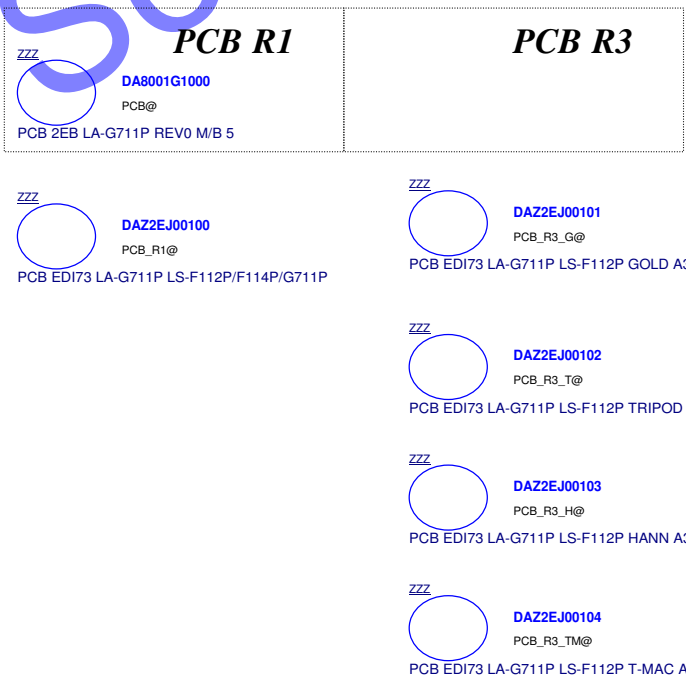
Screw hole/FD



FAN

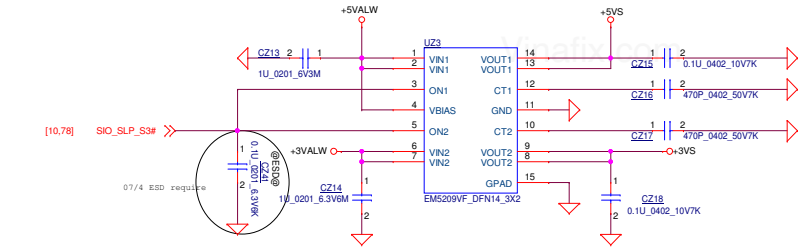


PCB PN

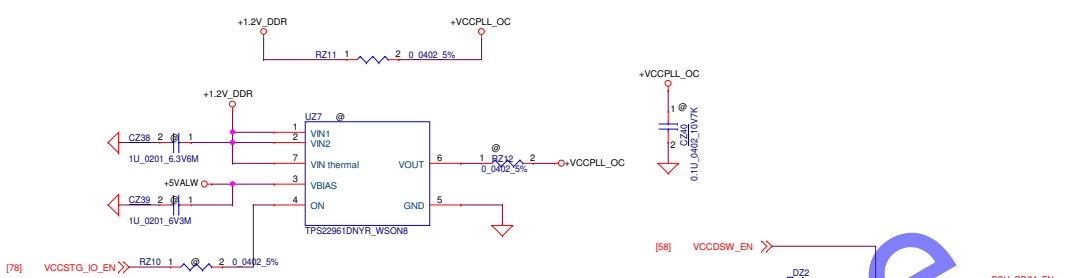


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Size		Document Number		Rev	
LA-G711P				0.2	
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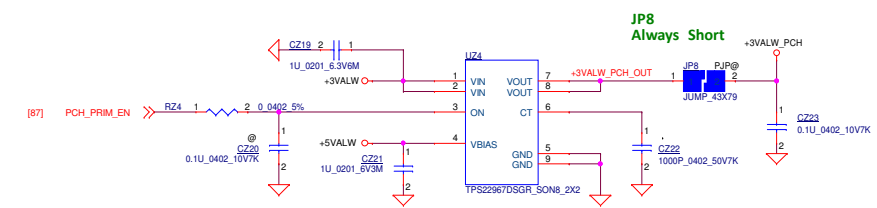
+5VS/+3VS for System



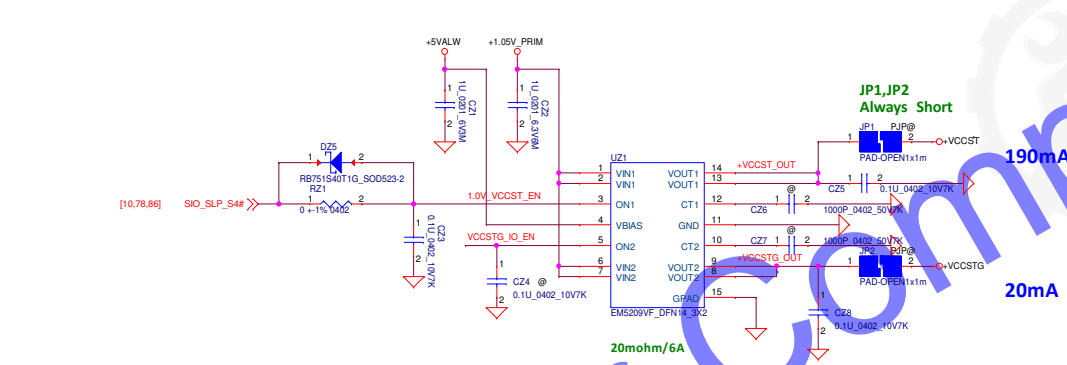
+VCCPLL_OC source



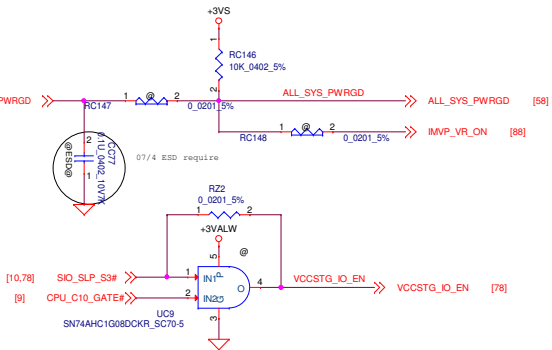
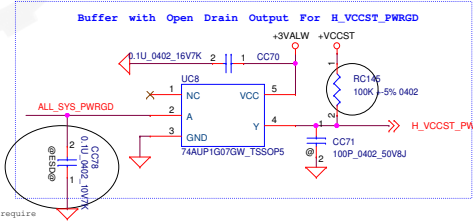
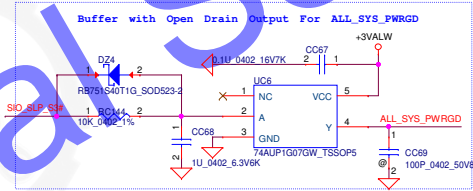
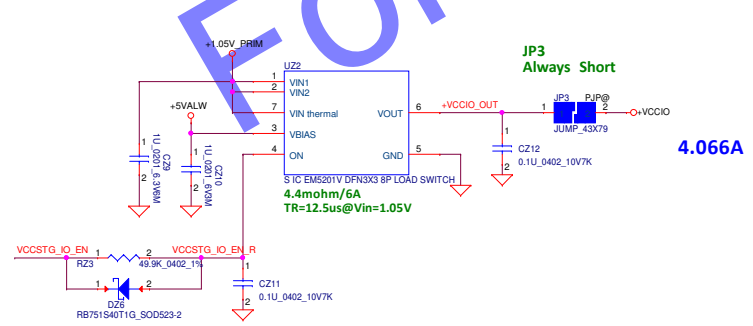
+3VALW_PCH for System



+1.05V_PRIM TO +VCCST /+VCCSTG

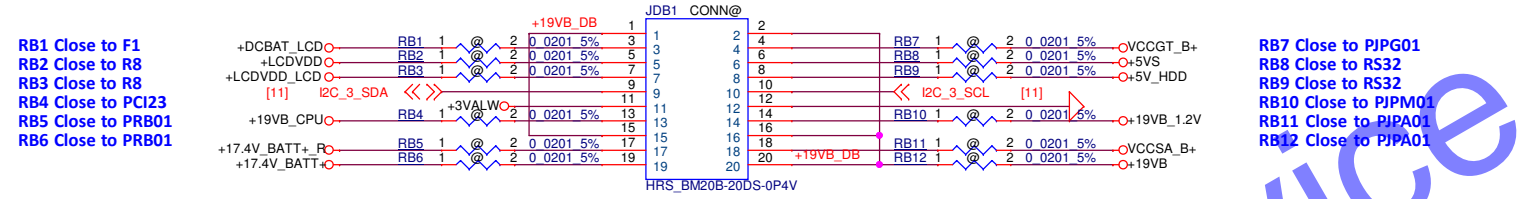


+1.05V_PRIM TO +VCCIO



Main Func = Power Monitor

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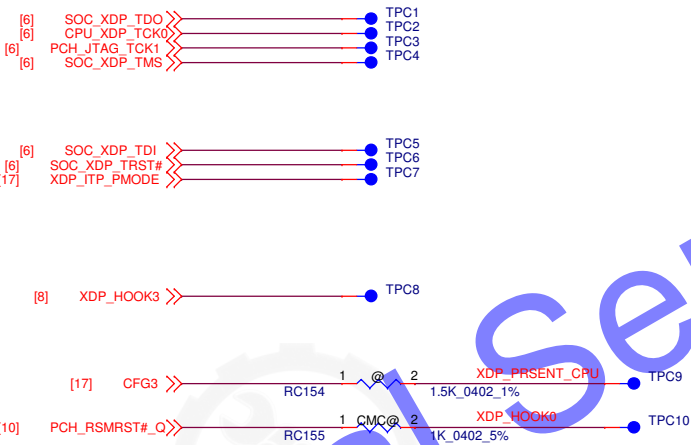
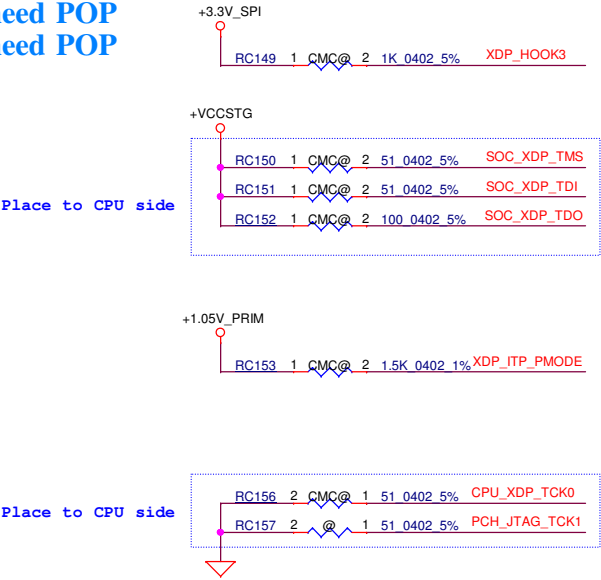


2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

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PortConnector Less Routing Topology

Follow KBL DCI Link
RC152 need POP
RC156 need POP




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Size	Document Number			Rev	
B	LA-G711P			0.2	
Date:		Wednesday, November 07, 2018		Sheet	80 of 101

Reserve

For Compal Service

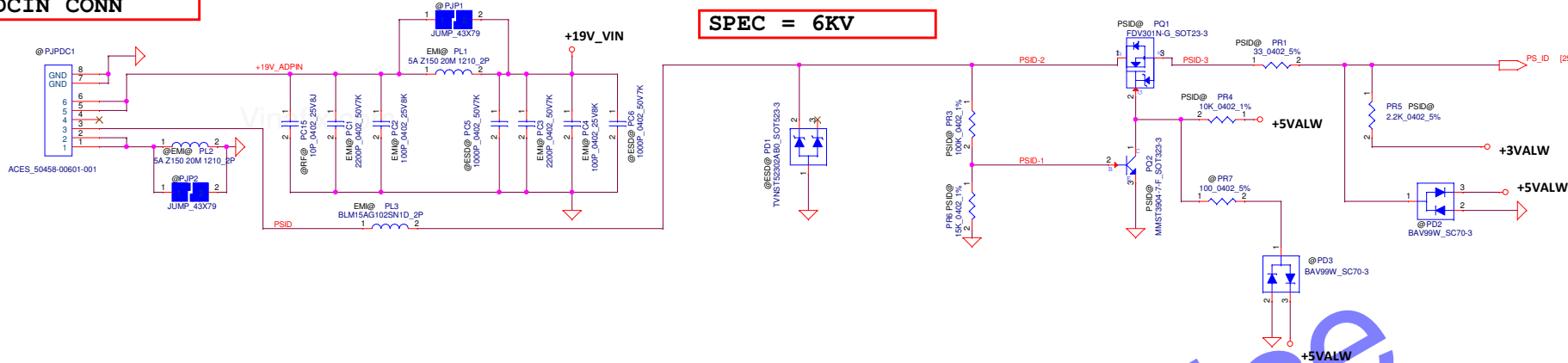
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		Compal Electronics, Inc.	
Title		Reserve for PWR	
Size	Document Number		Rev
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Main Func = DCIN CONN

SPEC = 6KV



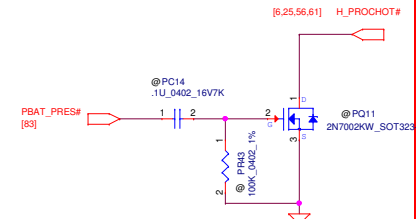
Bat tery Bat S de

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Bat t+
PIN9 Bat t+
PIN10 Bat t+
SP021412220

ACES_50458-01001-P01_10P-T

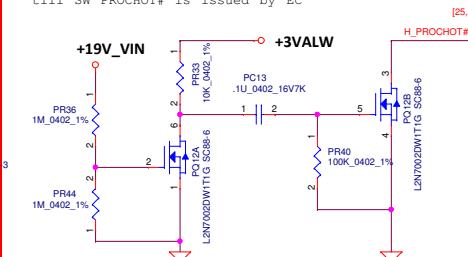
Adapter protection

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep e in BOM since battery can not
be removed by end user

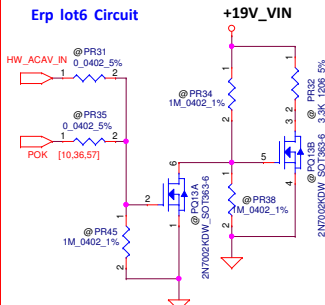


Battery protection

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW PROCHOT# is issued by EC



Erp lot6 Circuit



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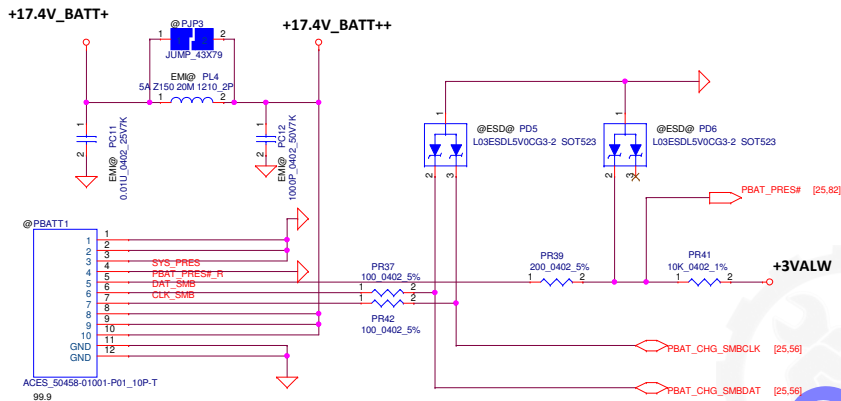
Security Classification	Compal Secret Data		Title	
Issued Date	2018/04/01	Deciphered Date	2019/04/01	PWR_DCIN CONN
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Bat tery Bat Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Bat t+
PIN9 Bat t+
PIN10 Bat t+
SP021412220

ACES_50458-01001-P01_10P-T



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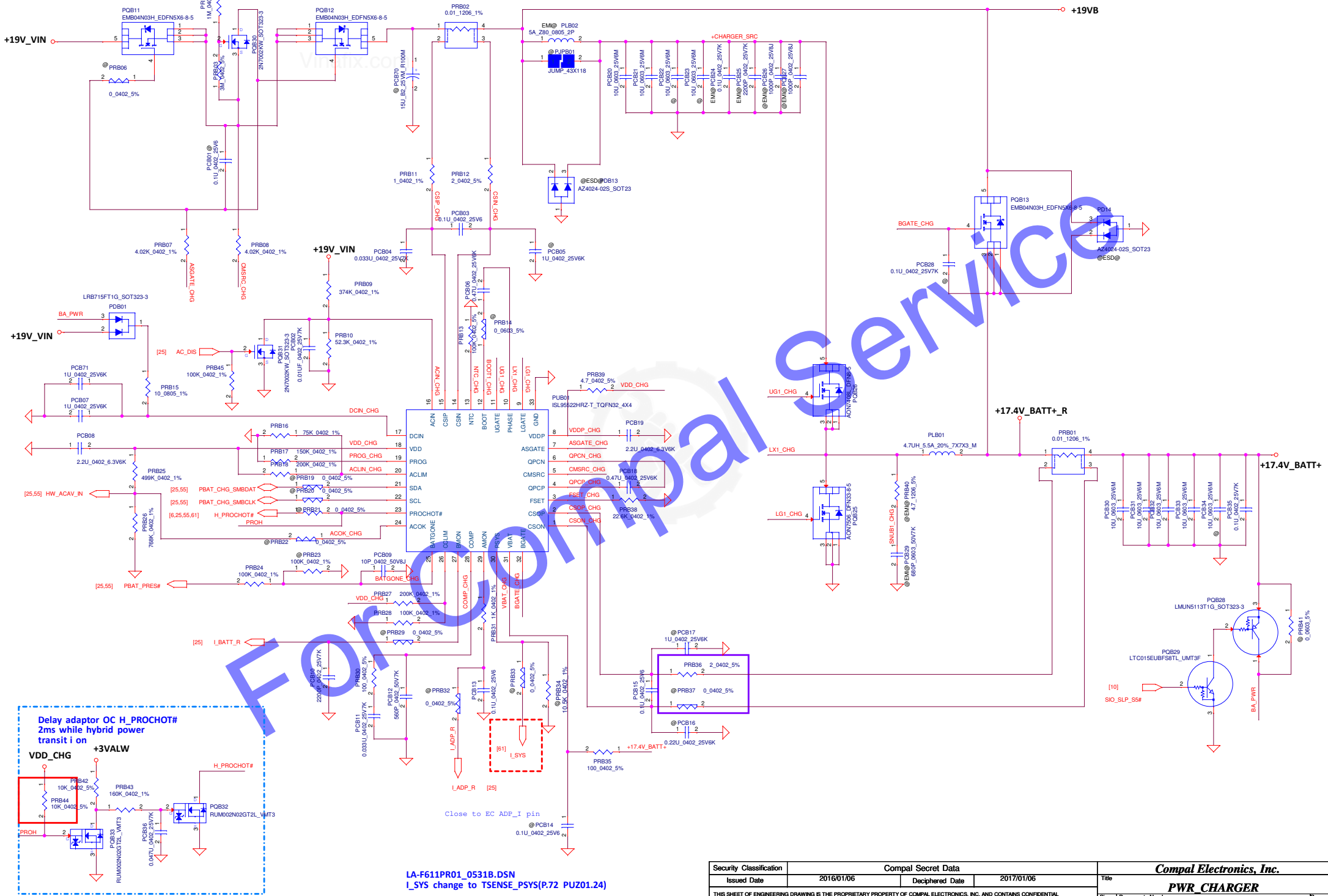
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PWR_BATT_CONN

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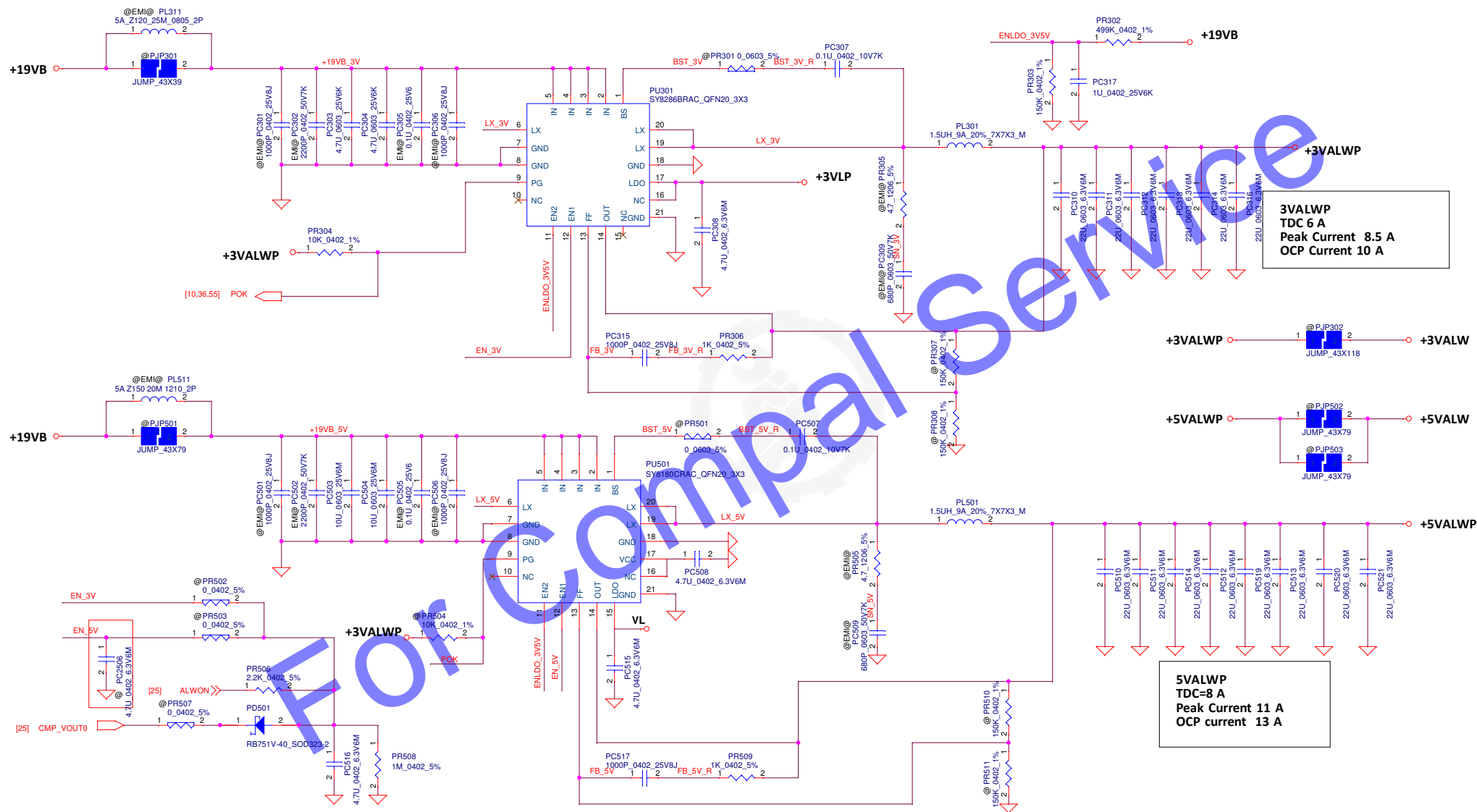
Main Func = CHARGER



LA-F611PR01_0531B.DSN
I_SYS change to TSENSE_PSYS(P.72 PUZ01.24)

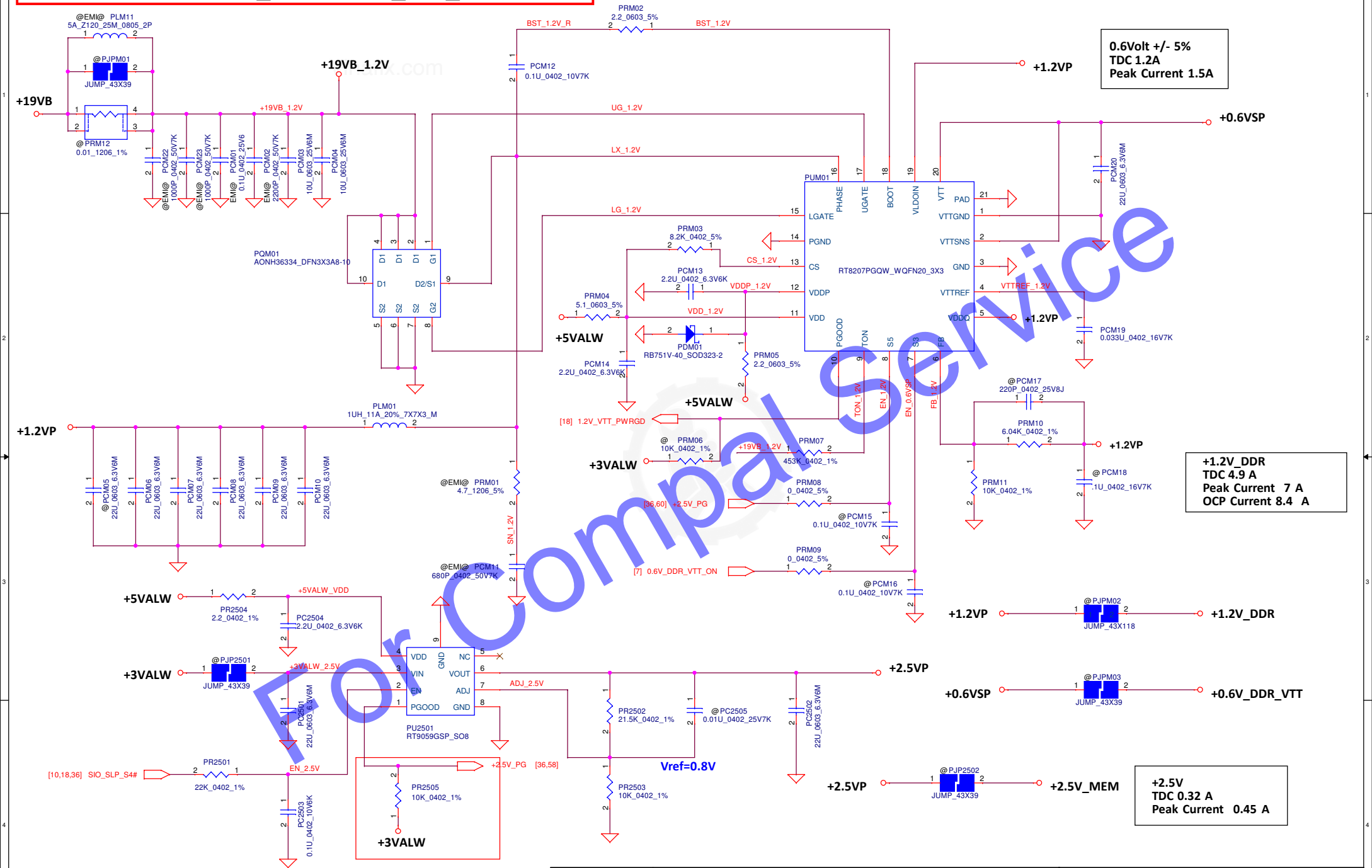
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					LA-F71IP	0.1
				Date:	Friday, November 23, 2016	Sheet 84 of 100

Main Func = 3.3VALWP/5VALWP



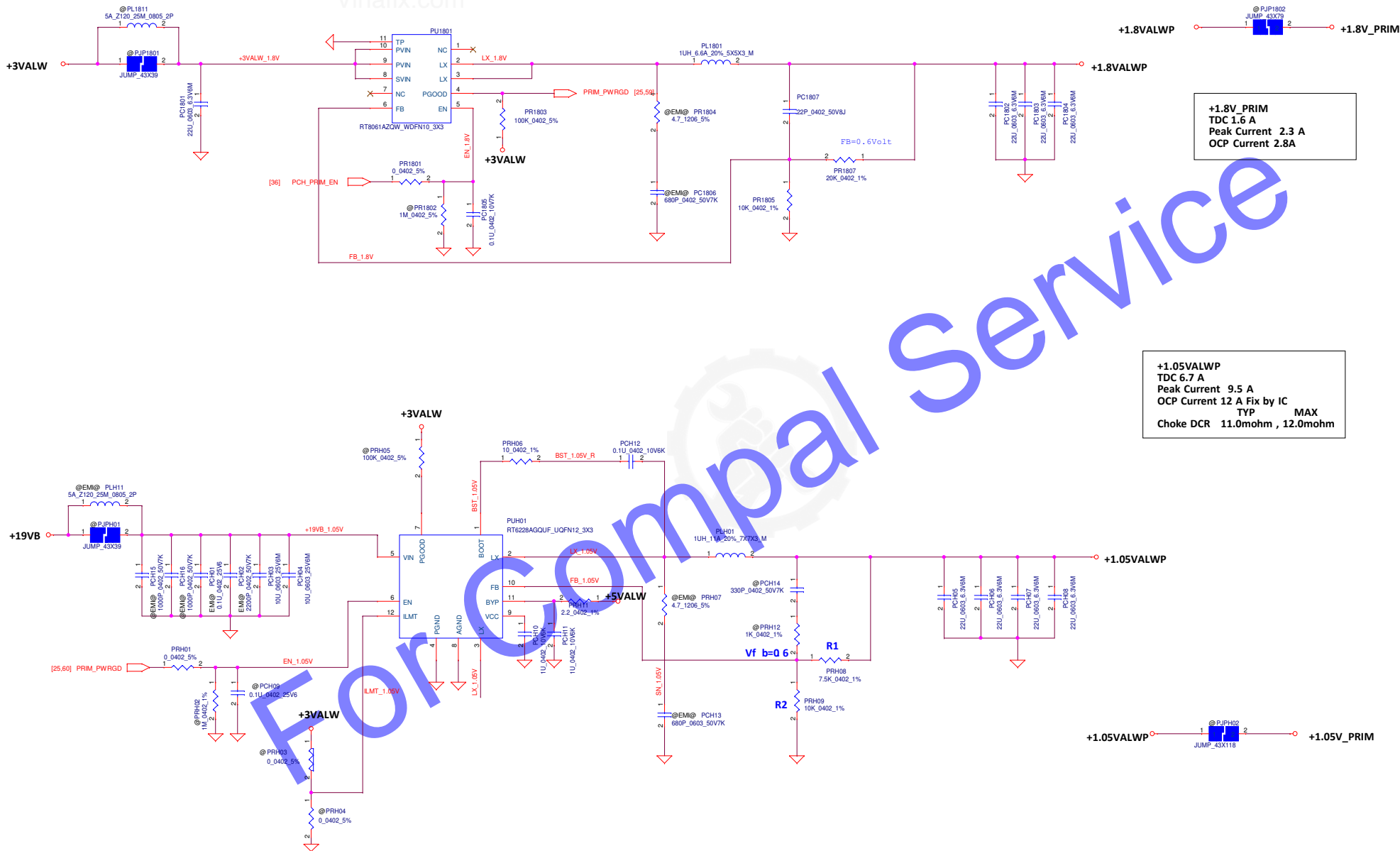
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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title		
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				Size	Document Number	Rev
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Main Func = +1.2V_DDR/+0.6V_DDR_VTT/+2.5VP



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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Size	Rev 0.1
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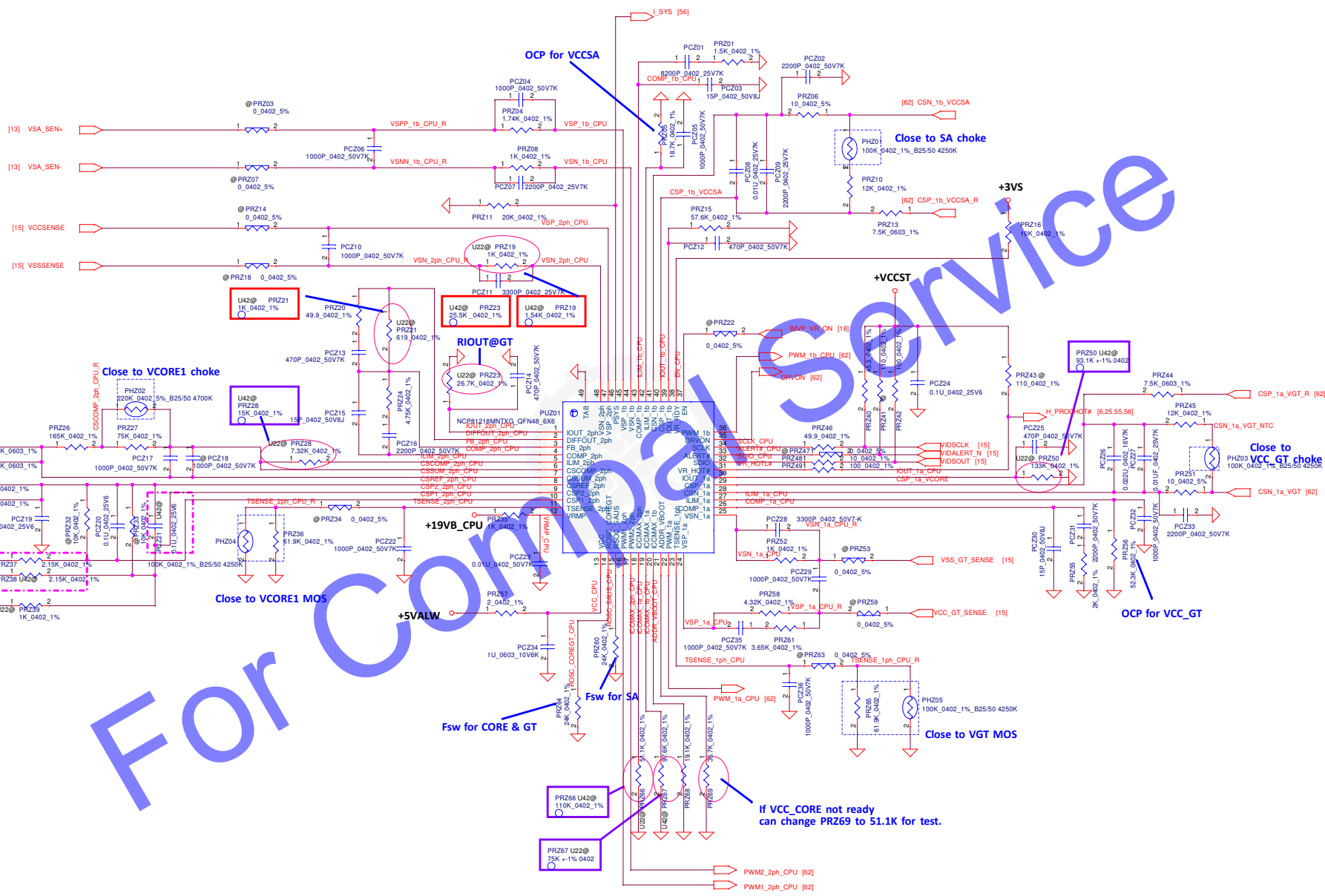
Main Func = +1.8VALWP /+1.05VALWP



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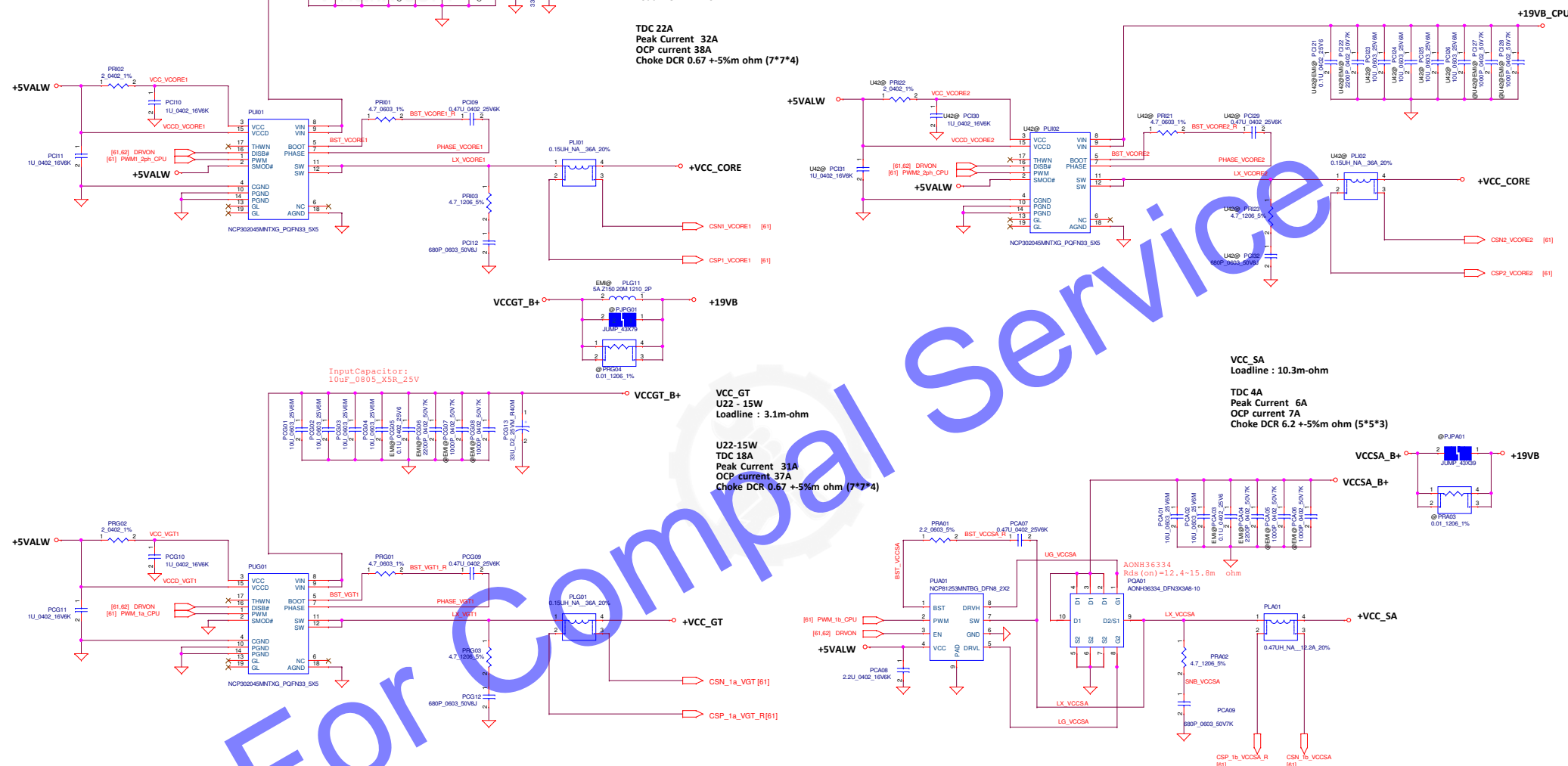
Main Func = CPU

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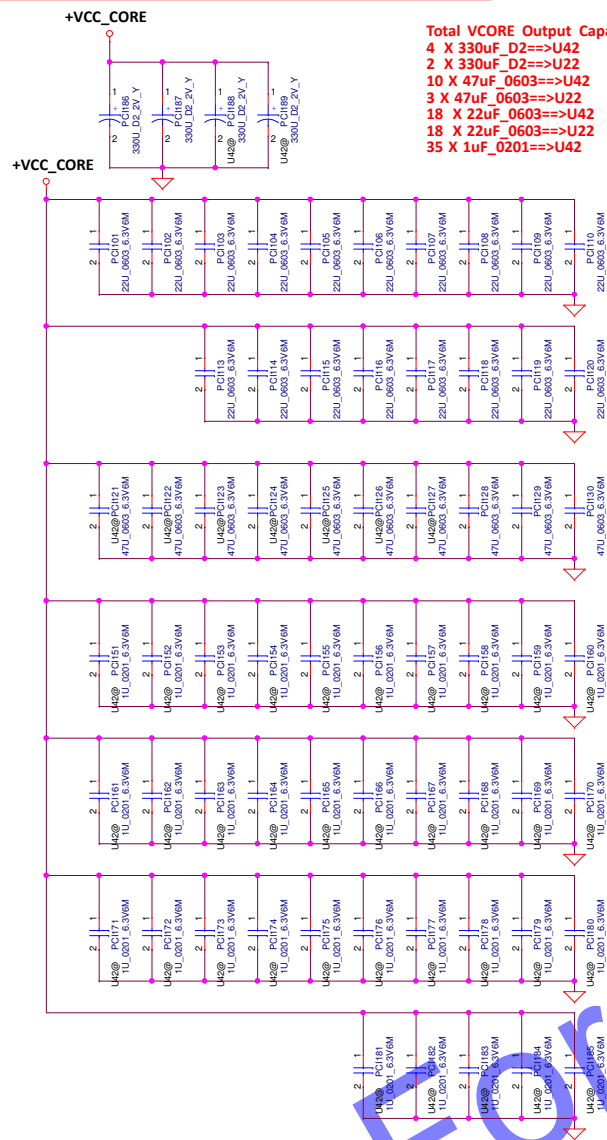
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Size	Document Number	Rev		Date: Friday, November 23, 2018	
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Main Func = CPUcore IA/GT/SA

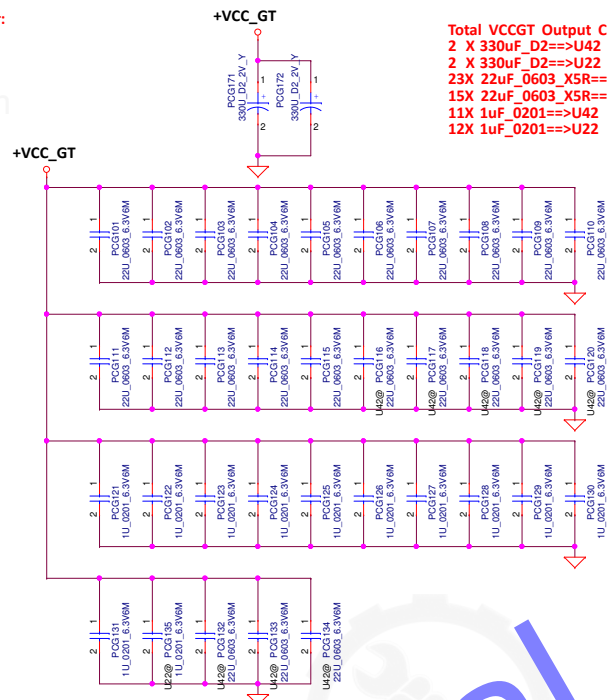


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Size	Document		rev 0.0	
Date:	Friday, November 28, 2018		Sheet	89 of 101

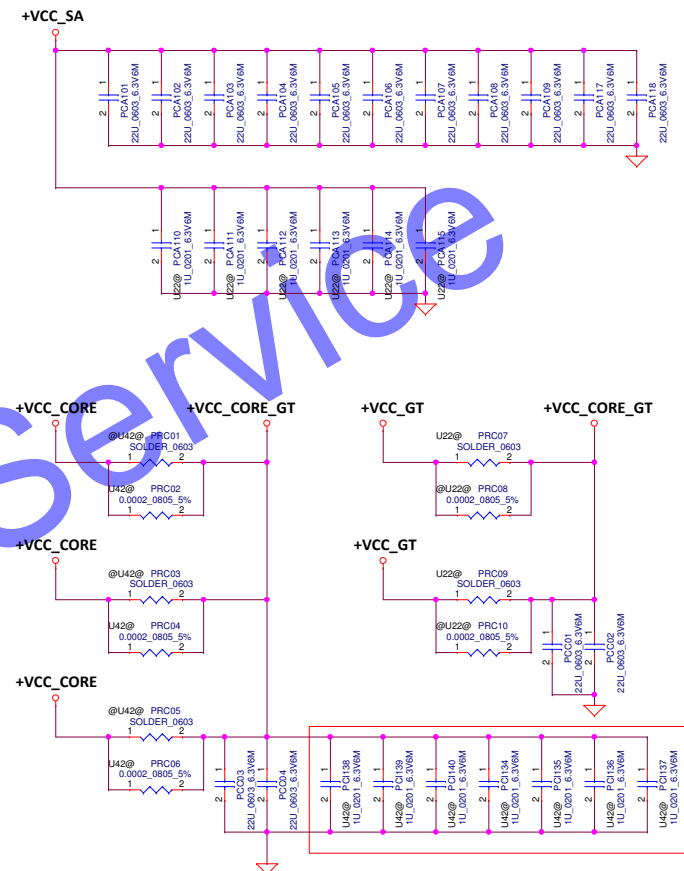
Main Func = CPU/ VGA / SA MLCC



Total VCORE Output Capacitor:
 4 X 330uF_D2==>U42
 2 X 330uF_D2==>U22
 10 X 47uF_0603==>U42
 3 X 47uF_0603==>U22
 18 X 22uF_0603==>U42
 18 X 22uF_0603==>U22
 35 X 1uF_0201==>U42



Total VCCGT Output Capacitor:
 2 X 330uF_D2==>U42
 2 X 330uF_D2==>U22
 23X 22uF_0603_X5R==>U42
 15X 22uF_0603_X5R==>U22
 11X 1uF_0201==>U42
 12X 1uF_0201==>U22




Total VCCSA Output Capacitor:
 11 X 22uF_0603==>U42
 11 X 22uF_0603==>U22
 6X 1uF_0201==>U22

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				Size	Document Number	Rev
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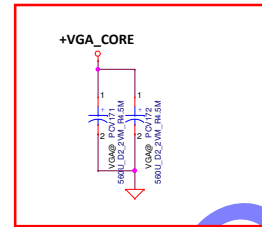
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	Size			Reserve for PWR		
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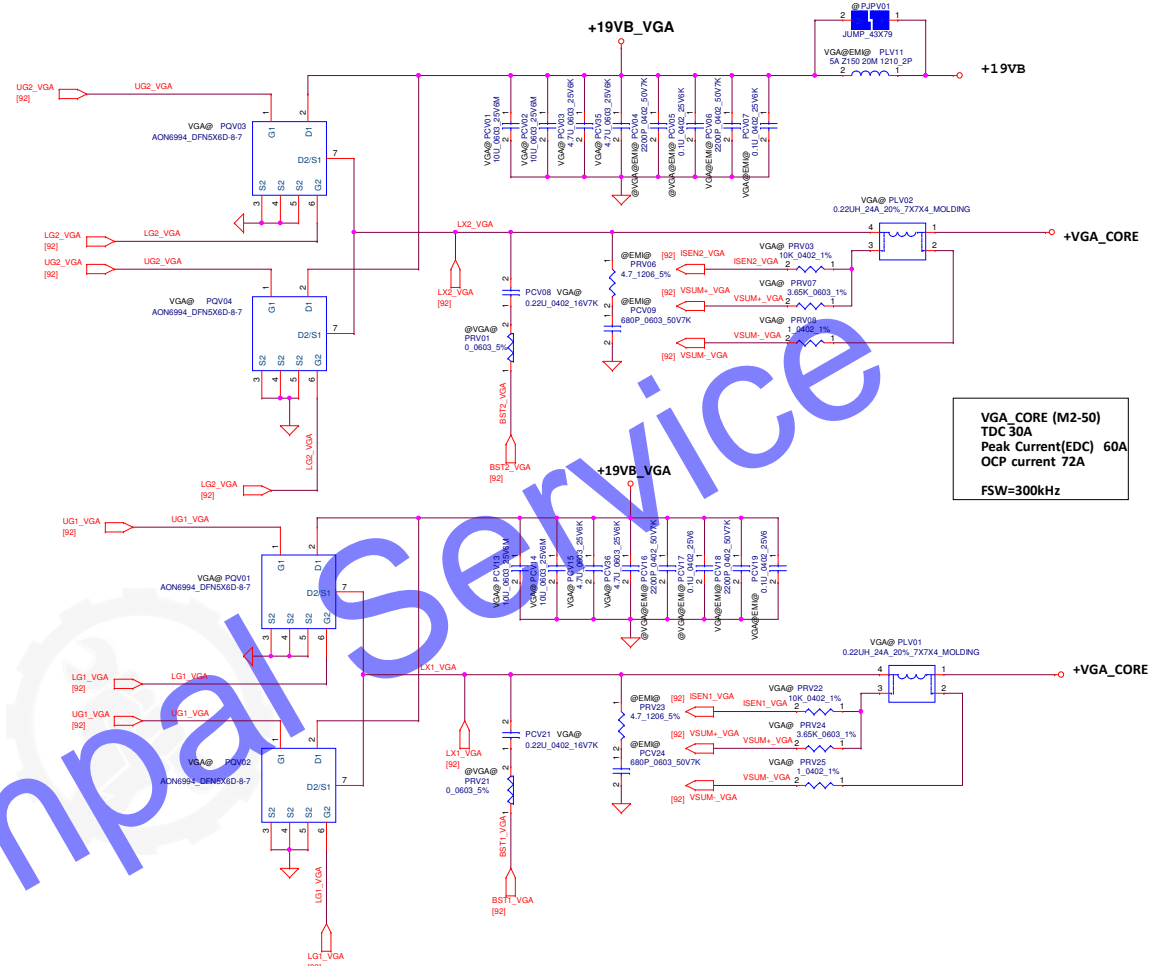
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Main Func = VGA CORE

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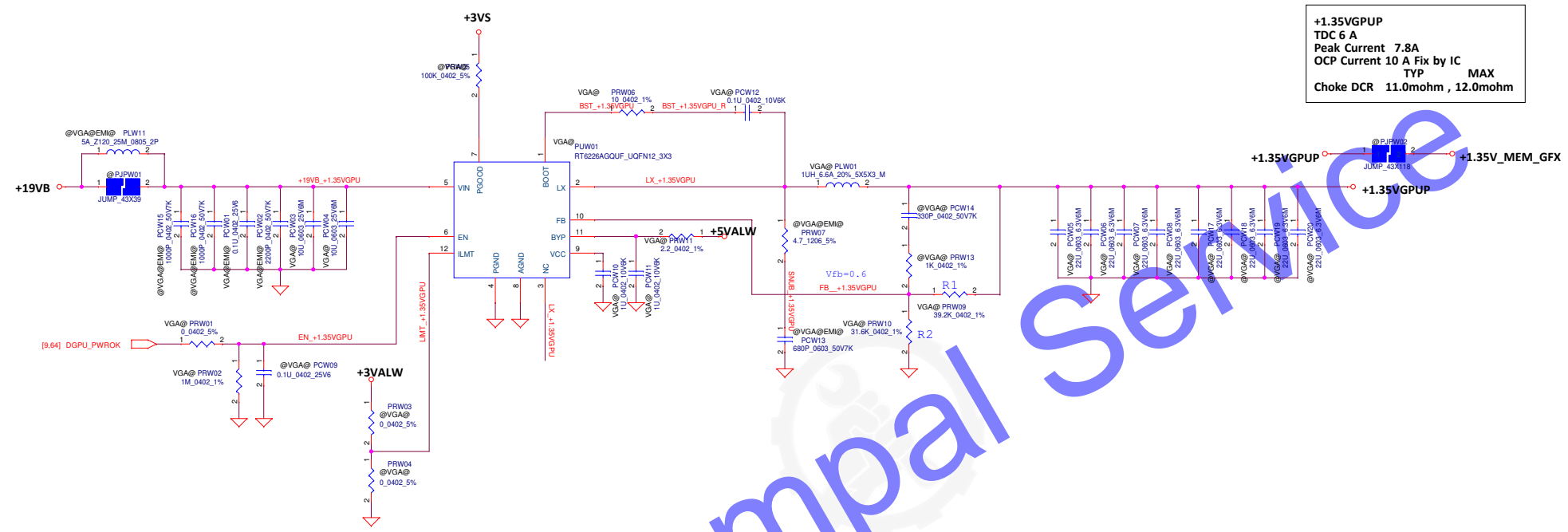
For VGACORE



VGA_CORE (M2-50)
TDC 30A
Peak Current(EDC) 60A
OCP current 72A
FSW=300kHz

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								GPU Decoupling	
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Main Func = +1.35VGPUP



+1.35VGPUP
TDC 6 A
Peak Current 7.8A
OCP Current 10 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm


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Reserve

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Version Change List (P. I. R. List)

Item	Page #	Date	Request Owner	Issue Description	Solution Description	Rev.
1.	P84-PWR_CHARGER	2018 06/12	Compal	Vendor suggest	Change the PRB11 from 20hm to 10hm	X01
2.	P84-PWR_CHARGER	2018 06/12	Compal	Downsize	Change the PCB06 and PCB18 to 0.47U_0402	X01
3.	P84-PWR_CHARGER	2018 06/12	Compal	Vendor suggest	Change the PCB11 to 0.33U	X01
4.	P89-PWR_CPU_Stage	2018 06/14	Compal	Downsize	PCA07, PCG09, PCI09, PCI29 change to 0.47U_0402	X01
5.	P92-PWR_VGA_CORE(ISL62771)	2018 06/14	Compal	Downsize	Change PCV30 to 0.15U_0402 Change PCV32 to 0.1U_0402	X01
6.	P86-PWR_1.2V_DDR	2018 07/05	Compal	Factory suggest	Change the PDM01 to SCS00000Z00	X01
7.	P83-BATT_CONN	2018 07/05	Compal	ESD request	Change the PD5,PD6 to SCA00002A00	X01
8.	P84-PWR_CHARGER	2018 07/09	Compal	Modify for AC detect	Change the PRB10 from 47K to 52.3K	X01
9.	P90-PWR_CPU MLCC	2018 07/09	Compal	Change for PI simulat i on	move PCI134,PCI135,PCI136,PCI137,PCI138, PCI139,PCI140 to +VCC_CORE_GT	X01
10.	P84-PWR_CHARGER	2018 07/11	Compal	Factory request	Add PCB71, PCB07 change to 1U_0402	X01
11.	P92-PWR_VGA_CORE	2018 07/17	Compal	Downsize	Change the PCV30 to SE000011G00 0.15U 16V	X01
12.	P88-PWR_CPU	2018 07/17	Compal	Change for CPU EA test	Change the PRZ25, PRZ29 to SD014100380 100K Change the PRZ23 to SD034255200 25.5K	X01

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	Compal Electronics, Inc.		
	Title PWR P.I.R		
	Size	Document Number	Rev 0.1
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Version Change List (P. I. R. List)

DVT1 EE change list

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout
Based on 05/15								
1	2018/5/17	8		Add RC207, CPU_SPL_0_CS#1	For 2nd ROM	Y	N	Y
2	2018/5/17	66		Del JP7, short +5VS and +5VS_ODD	Optimal B+ routing	Y	N	Y
3	2018/5/17	14		CC52,CC48,CC51,CS change to 0402	meet purchase requirement	Y	Y	Y
4	2018/5/17	29		CV73-CV78, CV100-CV109 change to 0402	meet purchase requirement	Y	Y	Y
5	2018/5/17	71		del CU3,CU8 CU4,CU9 IU change to 4.7U	meet purchase requirement	Y	Y	Y
6	2018/5/20			Del CS6,CU3,CU8; CU13,CU16,C8,C35,C39 change to 0201,CT1 change to 0603	MLCC downsize	Y	Y	Y
7	2018/5/25			Del C34,R68,R69,R70,R71; U2 change Footprint	For 17" Touch	Y	N	Y
8	2018/6/4	38		Connect UC1,CC30 to R72, Add RC208,RC209	For 17" Touch	Y	N	Y
9	2018/6/4			C27,CT14,CU10,CU11,CU5,CU6,CU17 change to 0603	MLCC downsize	Y	Y	Y
10	2018/6/4	31		CV161,CV162,CV163,CV164,CV165,CV166,CV167,CV168,CV169,CV170,CV182,CV183,CV184,CV185,CV186,CV187,CV188,CV189,CV190,CV191,CL16 change to 0201	MLCC downsize	Y	Y	Y
11	2018/6/13	56		CA16 change to 0402	MLCC downsize	Y	Y	Y
12	2018/7/4	65		add Rx10~14	co-lay ST TPM	Y	N	Y
13	2018/7/4			add CC75(pop),CZ41,CC76,CC77,CC78,CC79	For ESD requirement	Y	Y	Y
14	2018/7/6	65		add Rx15~RX19	co-lay China TPM	Y	N	Y

DVT2 EE change list

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout
Based on 07/16								
1	2018/8/14	66	RX20,RX21,RX22	reserve 0 ohm 0402	reserve for china TPM	Y	N	Y
2	2018/8/15	38	R96	reserve 0 ohm 0201	disconnct B+	Y	N	Y
3			EU1,EU3,EU8,EU9	SC300002C00=>SC300001Y00	ESD require	Y	Y	N
4		71	RE1	SD034178280=>SD034270280 17.8K change to 27K	EC board ID	Y	Y	N
5			CC54,CC57		fixed 1.05 OVPUBITS382716)	Y	Y	N
6			U22	SA00007XR00=>SA00008R600(Vccio load switch)	fixed 1.05 OVPUBITS382716)	Y	Y	N
7				Remove Typec configuration	Dell PCR	N	Y	N
8			CC64,CC52,CC59,CC17,CC15,CC18,CC19	0402 1u =>0201 1u	MLCC downsize	Y	Y	Y
9			R52	7.15K =>6.49K	Fixed OTP issue(BITS383003)	Y	Y	N